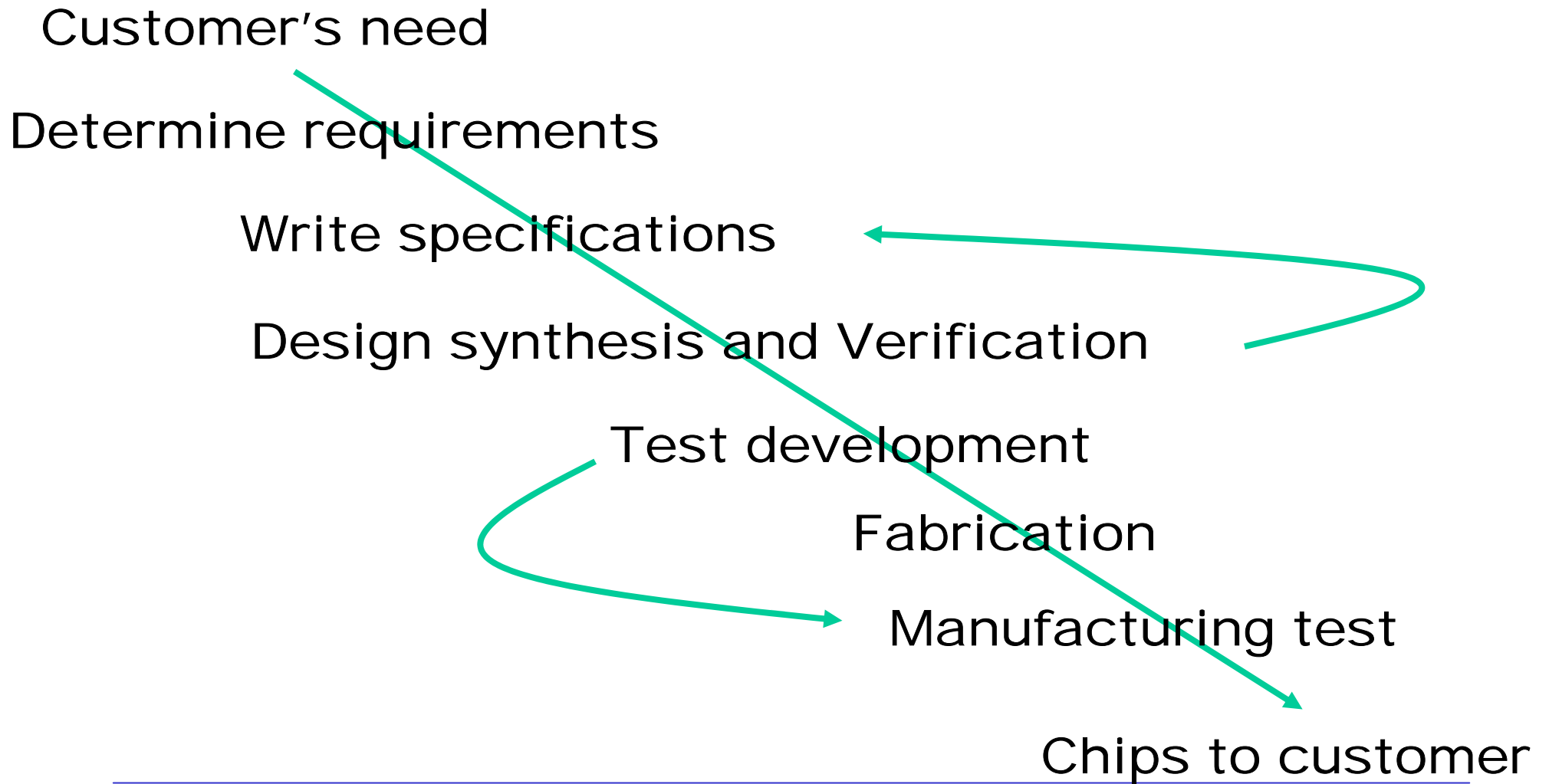
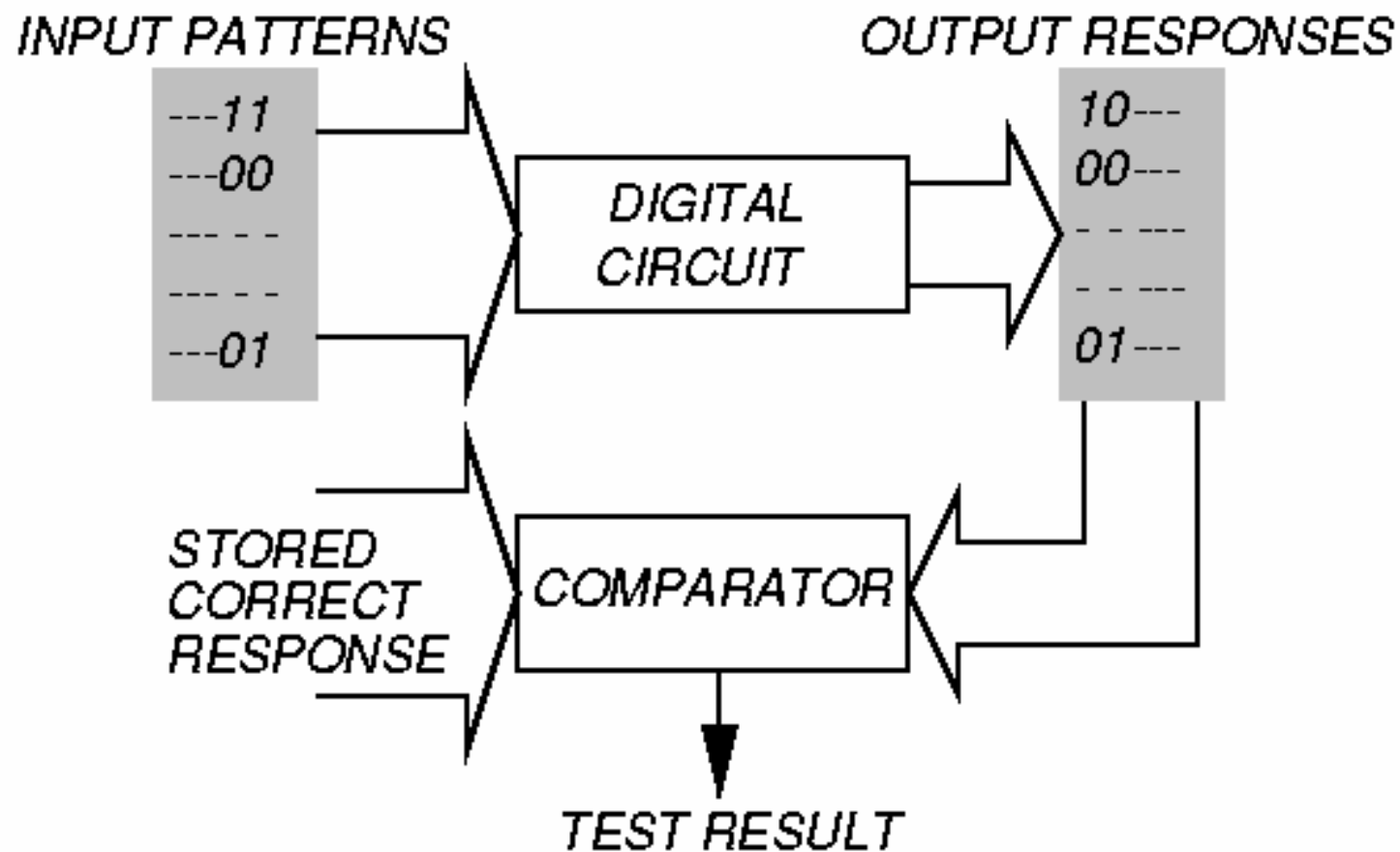

Il test di circuiti digitali

Introduction

VLSI Realization Process



Testing Principle



Levels of testing

□ Levels

- Chip
- Board
- System
 - Boards put together
 - System-on-Chip (SoC)
- System in field

□ Cost - Rule of 10

- It costs 10 times more to test a device as we move to higher level in the product manufacturing process

Cost of Manufacturing Testing in 2000AD

- ❑ 0.5-1.0GHz, analog instruments, 1024 digital pins: ATE purchase price
 - = $\$1.2\text{M} + 1,024 \times \$3,000 = \$4.272\text{M}$
- ❑ Running cost (five-year linear depreciation)
 - = Depreciation + Maintenance + Operation
 - = $\$0.854\text{M} + \$0.085\text{M} + \$0.5\text{M}$
 - = $\$1.439\text{M}/\text{year}$
- ❑ Test cost (24 hour ATE operation)
 - = $\$1.439\text{M} / (365 \times 24 \times 3,600)$
 - = 4.5 cents/second

Il test di circuiti digitali

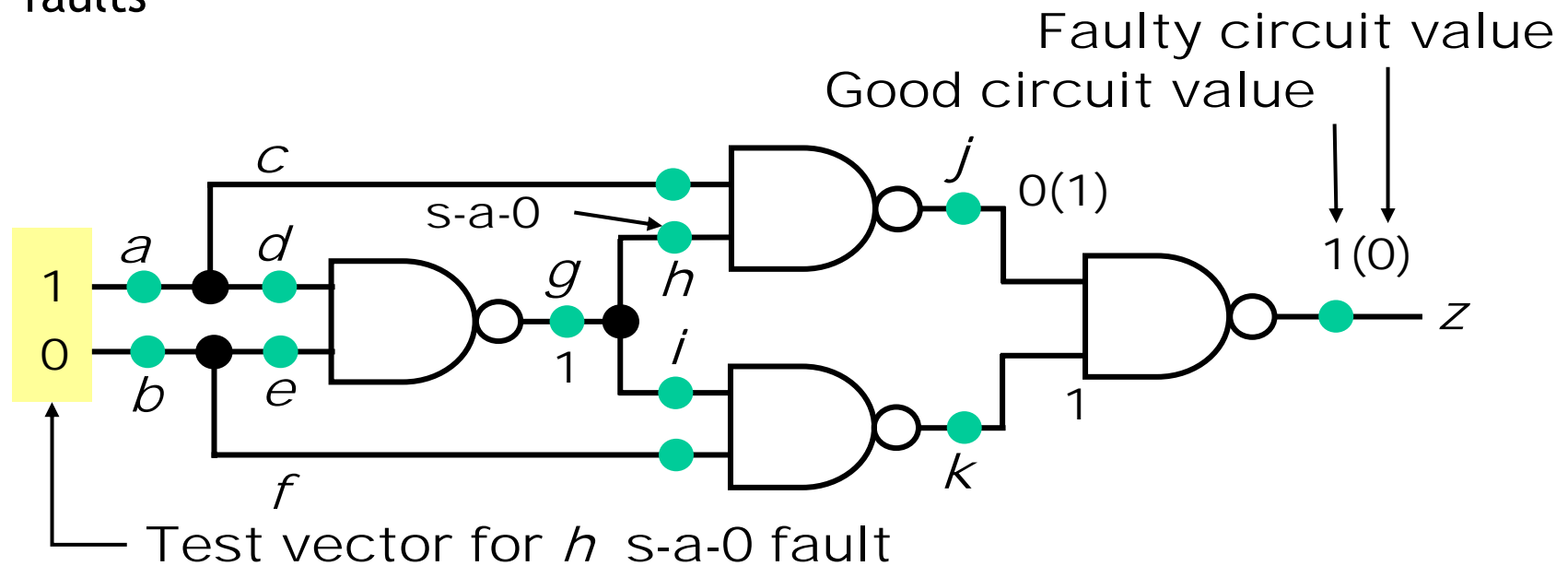
Fault Modeling

Stuck-at Faults

- ❑ Single stuck-at faults
- ❑ What does it achieve in practice?
- ❑ Fault equivalence
- ❑ Fault dominance and checkpoint theorem
- ❑ Classes of stuck-at faults and multiple faults

Single Stuck-at Fault

- Three properties define a single stuck-at fault
 - Only one line is faulty
 - The faulty line is permanently set to 0 or 1
 - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults



Single Stuck-at Faults (contd.)

- How effective is this model?
 - Empirical evidence supports the use of this model
 - Has been found to be effective to detect other types of faults
 - Relates to yield modeling
 - Simple to use

Il test di circuiti digitali

Fault Simulation

Problem and Motivation

❑ Fault simulation Problem: Given

- A circuit
- A sequence of test vectors
- A fault model
- Determine
 - Fault coverage - fraction (or percentage) of modeled faults detected by test vectors
 - Set of undetected faults

❑ Motivation

- Determine test quality and in turn product quality
- Find undetected fault targets to improve tests

Fault Simulator in a VLSI Design Process

