

Pomante Luigi

Curriculum Vitae (last update 7th August 2010)

GENERAL INFORMATION

First Name	Luigi
Surname	Pomante
Date of birth	1 st October, 1972
Place of birth	Giulianova (Italy)
Nationality	Italian
Contacts	luigi.pomante@univaq.it, luigi@pomante.net
Personal Site	www.pomante.net

MAIN ACTIVITIES

Since November 2008

Assistant Professor & Academic Researcher

- *Center of Excellence DEWS*
 - o *Architecture and Design of Embedded controllers, Wireless interconnect and System-on-chip*
 - *University of L'Aquila (ITALY)*

May 2008 – October 2008

Research grant

- *Center of Excellence DEWS*

Since 1999

R&D Consultant

- Since 2006: *WEST Aquila (SME)*
 - o *Wireless Embedded Systems Technologies c/o University of L'Aquila*
- January 2006 - April 2008: *Center of Excellence DEWS*
- July-December 2005: *Department of Electrical and Information Engineering*
 - o *University of L'Aquila – Faculty of Engineering*
- July 1999 - June 2005: *Center of Excellence CEFRIEL*
 - o *Digital Technologies and Operating Systems Unit - Politecnico di Milano (ITALY)*

Lecturer

- *Politecnico di Milano, University of L'Aquila, CEFRIEL, Industrial education*

Advisor and Tutor for thesis

- *Politecnico di Milano, CEFRIEL, University of L'Aquila, DEWS*

2001

Ph.D. in Computer Science Engineering

- *Politecnico di Milano*

1999

M.S. in Information Technology

- *CEFRIEL*

1998

Registered engineer qualification

- *Politecnico di Milano*

Degree in Computer Science Engineering

- *Politecnico di Milano*

EDUCATION

2001

Ph.D. in Computer Science Engineering

- *Politecnico di Milano - DEI*

Thesis: “*System-Level Co-Design of Heterogeneous Multiprocessor Embedded Systems*”
[TH.3]

1999

M.S. in Information Technology

(100/100 L)

- *CEFRIEL*

ICT Center of Excellence For Research, Innovation, Education and industrial Labs partnership, Via Fucini 2, 20133, Milano

Thesis (italian): “*Co-Simulazione HW/SW a livello di sistema*”

[TH.2]0

1998

“Laurea” Degree in Computer Science Engineering

(83/100)

- *Politecnico di Milano - DEI*

Thesis (italian): “*La qualità dei dispositivi con proprietà di autodiagnosi: una metodologia di valutazione innovativa*”

[TH.1]

1991

High school degree “Industrial Computer Science Technician”

(58/60)

- *I.T.I.S. “G. e M. Montani”, Fermo (AP), ITALY*

TEACHING ACTIVITIES

ACADEMIC

Since 2008

Faculty of Engineering, University of L'Aquila
"Embedded Systems" course

Since 2005

Faculty of Engineering, University of L'Aquila
Lectures on "Wireless Sensor Networks" in several courses

2003-2005

Politecnico di Milano
"Computer Science" course
"Industrial Computer Science" course

1999-2004

Politecnico di Milano
"Computer Science" course (assistant)
"Computer Architectures" course (assistant)
"Operating Systems" course (assistant)

1998-1999

Politecnico di Milano
"Computer Science" course (tutor)

CEFRIEL CENTRE

1999-2005

Lectures on VLSI Design: Introduction to SystemC
Lectures on UNIX
Lectures on Computer Architectures and Operating Systems

INDUSTRY

2002-2007

Lectures on UNIX/Linux
Lectures on EDP
Lectures on CAD
Lectures on Operating Systems
Lectures on Computer Architectures and Operating Systems
Lectures on C/C++

MAIN RESEARCH ACTIVITIES

Multiprocessor Systems for Real-Time Applications

[RP.1]

System-Level HW/SW Co-Design of Multiprocessor Embedded Systems

[TH.2][TH.3]

[IC.12][IC.18][IC.7][IC.2][IC.11][JR.4][IC.22][IC.5][JR.1][IC.29][IC.31] [IC.35]

Estimation and Optimization of SW Power Consumption

[IC.3][IC.20][JR.5]

Quality Analysis of Self-Checking Devices

[TH.1]

[IC.1] [JR.3]

System-Level HW/SW Concurrent Error Detection

[RP.2]

[IC.6][IC.8][IC.4][JR.2][IC.16][IC.17]

System-Level Object-Oriented Specifications

[RP.3]

[IC.9][BK.1][IC.10][IC.13][IC.14][IC.15]

Dedicated HW/SW Architectures for DBMS

[IC.19][IC.21][JR.6][IC.26][IC.30]

Wireless Sensor Networks

[IC.23][IC.24][IC.25][BK.2][IC.27][JR.7][IC.24][IC.28][BK.3][IC.32][IC.33][IC.34]

OTHER RELEVANT ACTIVITIES

2010

TPC Member: *8th Annual IEEE Consumer Communications and Networking Conference - Smart Spaces and Personal Area Networks (CCNC 2011)*.

2008

TPC Member: *2nd International Conference on Signals, Circuits & Systems (SCS 2008)*.

1999-2010

Reviewer for several international journals and conferences

Advisor and Tutor for thesis

RESEARCH PROJECTS

1999-2010

Involvement in the following European Research Projects:

[EP.1] **ESPRIT Project N. 22133 – SEED**

[EP.2] **IST Project N. 1999-11476 - ODETTE**

[EP.3] **IST Project N. 2000-30125 - POET**

[EP.4] **IST Project N. 2004-511368 - HYCON**

[EP.5] **ERC-2009-StG 240555-VISION**

1999-2010

Involvement in near 10 Industrial Research Projects related to CEFRIEL, DEWS and WEST Aquila about Wireless Networked Embedded Systems.

PUBLICATIONS

INTERNATIONAL CONFERENCES

- [IC.1] with D. Sciuto, C. Bolchini, F. Salice. "A Synthesis methodology aimed at improving the quality of TSC devices", *Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI System* (IEEE DFT 1999).
- [IC.2] "Co-design of Multiprocessor Embedded Systems: an Heuristic Multi-Level Partitioning Methodology", *Proceedings on IFIP International Conference on Chip Design Automation* (IFIP ICDA 2000).
- [IC.3] with D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "A Multi-Level Strategy for Software Power Estimation", *Proceedings of IEEE International Symposium on System Synthesis* (IEEE ISSS 2000).
- [IC.4] with D. Sciuto, F. Salice, C. Bolchini. "Reliability properties Assessment at System Level: A Co-Design Framework", *Proceedings of 7th IEEE International On-Line Testing Workshop* (IEEE IOLTW 2001).
- [IC.5] with D. Sciuto, F. Salice, W. Fornaciari. "HW/SW Timing Simulation Environment for Multiprocessor Embedded Systems", *5th World Multi-Conference on Systemics, Cybernetics and Informatics* (SCI 2001).
- [IC.6] with D. Sciuto, F. Salice, C. Bolchini. "On-Line Fault Detection in a Hardware/Software Co-design Environment: System Partitioning", *Proceedings of 14th IEEE/ACM International Symposium on System Synthesis* (IEEE/ACM ISSS 2001).
- [IC.7] with W. Fornaciari, F. Salice, D. Sciuto. "Metrics for Design Space Exploration of Heterogeneous Multiprocessor Embedded System", *IEEE/ACM International Workshop on Hardware Software Co-Design* (IEEE/ACM CODES 2002).
- [IC.8] with C. Bolchini, F. Salice, D. Sciuto. "A System Level Approach in Designing Dual-Duplex Fault Tolerant Embedded Systems", *IEEE International On-Line Testing Workshop* (IEEE IOLTW 2002).
- [IC.9] with W. Fornaciari, M. Bombana. "SystemC-Plus Complex Data Type for Telecom Applications", *Proceedings of Forum on Specification and Design Languages* (FDL 2002).
- [IC.10] with M. Bombana. "SystemC-Based Library Approach for Data-intensive Applications", *Conference on Design of Circuits and Integrated Systems* (DCIS 2002).
- [IC.11] with W. Fornaciari, F. Salice, L. Del Vecchio. "Partitioning of Embedded Applications onto Heterogeneous Multiprocessor Architectures", *ACM Symposium on Applied Computing* (ACM SAC 2003).
- [IC.12] with F. Salice, W. Fornaciari, D. Sciuto. "An Internal Representation Model for System-Level Co-Design of Heterogeneous Multiprocessor Embedded System", *Forum on Specification and Design Languages* (FDL 2003).
- [IC.13] with R. Farina, L. Pizzamiglio. "System Design using SystemC-Plus: A Case Study in the Telecom Domain", *International Conference on Cybernetics and Information Technologies, Systems and Applications* (CITSA 2004).
- [IC.14] with R. Farina, L. Pizzamiglio, "Experimenting Object-Oriented System-Level Design in the ATM domain", *Forum on Specification and Design Languages* (FDL 2004).
- [IC.15] "Exploiting Polymorphism in the HW Design: a Case Study in the ATM Domain", *CODES+ISSS 2004*.
- [IC.16] with A. Miele, F. Salice, C. Bolchini, D. Sciuto, "Reliable System Co-Design: the FIR Case Study", *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT 2004).
- [IC.17] with F. Salice, C. Bolchini, D. Sciuto, "Reliable System Specification for Self-Checking Data-Paths", *Design, Automation and Test in Europe – Conference & Exhibition* (DATE 2005).
- [IC.18] with C. Brandolese, D. Scarpazza, P. Di Felice, "Parsing SystemC: an open-source, easy to extend parser", *IADIS Applied Computing Conference*, 2006.
- [IC.19] with P. Di Felice, "Integration of Spatial Data Types and Operators into Relational DBMSs: A Survey", *IADIS Applied Computing Conference*, 2006.

- [IC.20] with C. Brandolese, W. Fornaciari, F. Salice, R. Zafalon, "DPM at OS level: low-power scheduling policies", *5th WSEAS International Conference on CIRCUITS, SYSTEMS, ELECTRONICS, CONTROL & SIGNAL PROCESSING (CSECS '06)*.
- [IC.21] with P. Di Felice, "Ad-hoc HW/SW Architectures for DBMSs: a Co-Design Approach", *WSEAS International Conferences 2007 (AIKED, SEPADS, EHAC and ISPRA)*, 2007.
- [IC.22] with F. Graziosi, L. Imbriglio, "Topology-aware System Design Exploration for Embedded Applications implemented onto Heterogeneous Multiprocessor SoC", *IEEE International Conference on Design & Technology of Integrated Systems (DTIS2008)*.
- [IC.23] with P. Di Felice, M. Ianni. "A spatial extension of TinyDB for wireless sensor networks", *IEEE Symposium on Computers and Communications (ISCC'08)*.
- [IC.24] with F. Graziosi, F. Santucci, C. Rinaldi, S. Tennina, C. Fischione. "Mining Ventilation Control: Wireless Sensing, Communication Architecture and Advanced Services". *4th Annual IEEE Conference on Automation Science and Engineering (CASE 2008)*.
- [IC.25] with F. Graziosi, C. Rinaldi. "Exploiting WSN for audio surveillance applications: the VoWSN approach", *11th IEEE Euromicro Conference on Digital System Design (DSD'08)*.
- [IC.26] "A System-Level Co-Design Methodology for DBMS-Specific Architectures", *11th IEEE Euromicro Conference on Digital System Design (DSD'08, WIP-SS)*.
- [IC.27] with F. Graziosi, D. Pacifico. "A Middleware-Based Approach for Heterogeneous Wireless Sensor Networks". *The 12th WSEAS International Conference on COMMUNICATIONS (part of the 12th WSEAS CSCC Multiconference)*.
- [IC.28] with S. Tennina, F. Graziosi, M. Di Renzo, R. Alesii, F. Santucci. "Localization, tracking, and automatic personal identification in GPS-denied environments: a solution based on a wireless biometric badge", *5th ICST/IEEE/ACM TridentCom*, 2009.
- [IC.29] with F. Graziosi, L. Imbriglio. "Application-Specific System-Level Design Space Exploration for Heterogeneous Multiprocessor Embedded Platforms". *DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications*.
- [IC.30] with P. Di Felice. "Ad-hoc Architectures for modern DBMS: a HW/SW Co-Design Approach". *DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications*.
- [IC.31] with F. Graziosi, L. Imbriglio. "System-Level Design Space Exploration for Application-Specific HW/SW Systems". *2009 IEEE Toronto International Conference-Science and Technology for Humanity (TIC-STH 2009): Symposium on Electronic Design Automation*.
- [IC.32] with S. Tennina, F. Graziosi, M. Di Renzo, R. Alesii, F. Santucci. "Distributed Localization, Tracking, and Automatic Personal Identification: A Solution based on a Wireless Biometric Badge". *4th ACM Int. Workshop on Wireless Network Testbeds, Experimental Evaluation and Characterization*, 2009.
- [IC.33] with S. Tennina, F. Graziosi, M. Di Renzo, R. Alesii, F. Santucci. "Integrated GPS-denied Localization, Tracking and Automatic Personal Identification". *7th ACM Conf. on Embedded Networked Sensor Systems*, 2009.
- [IC.34] with F. Santucci, M. Pugliese. "Agent-based Scalable Design of a Cross-Layer Security Framework for Wireless Sensor Networks Monitoring Applications". *IEEE International Workshop on Scalable Ad Hoc and Sensor Networks*, 2009.
- [IC.35] "System-Level Design Space Exploration for HMPSoC". *3rd Workshop on Mapping of Applications to MPSoCs by The ArtistDesign European Network of Excellence*, 2010.
- [IC.36] with C. Rinaldi, F. Graziosi. "RF Sounding: listening the cellphone", *7th International Symposium on Computer Music Modeling and Retrieval*, 2010.

BOOK CHAPTERS

- [BK.1] with W. Fornaciari, M. Bombana. "SystemC-Plus Complex Data Type for Telecom Applications", *System Specification and Design Languages (best of FDL'02)*, CHDL Series, Kluwer, 2003, pp. 219-229.
- [BK.2] with R. Alesii, G. Gargano, F. Graziosi, C. Rinaldi. "WSN-based Audio Surveillance Systems", *SPRINGER VERLAG Book - Springer Verlag Lecture Notes Series*, 2009.
- [BK.3] with S. Tennina, F. Graziosi, M. Di Renzo, R. Alesii, F. Santucci. "Integrated GPS-denied Localization, Tracking and Automatic Personal Identification". *20th Tyrrhenian International Workshop on Digital Communications, Springer Book Series 2009*.

INTERNATIONAL JOURNALS

- [JR.1] with D. Sciuto, F. Salice, W. Fornaciari. "Hw/Sw Cosimulation for Fast Design Space Exploration of Multiprocessor Embedded Systems", *Canadian Journal of Electrical and Computer Engineering (CJECE)*, vol. 26, n. 3/4, July/October 2001, pp.135-140.
- [JR.2] with C. Bolchini, F. Salice, D. Sciuto. "Reliability Properties Assessment at System Level: a Co Design Framework", *Journal of Electronic Testing - Theory and Application (JETTA)*, Kluwer Academic Publishers, The Netherlands, Vol. 18, no. 3, p. 351-356, 2002 (ISSN 0923-8174)
- [JR.3] with C. Bolchini, F. Salice, D. Sciuto. "The Design of Reliable Devices for Mission Critical Applications", *IEEE Trans. on Instrumentation and Measurement (TIM)*, Vol. 52, no. 6, pp. 1703-1712, 2003 ISSN:0018-9456/03.
- [JR.4] with D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC", *IEEE Transactions on Computers*, vol. 55, no. 5, May 2006.
- [JR.5] With C. Brandolese, W. Fornaciari, F. Salice, R. Zafalon, "Energy Aware Scheduling of Processes at OS Level", *WSEAS Transactions on CIRCUITS and SYSTEMS*, Issue 12, Vol. 5, December 2006, ISSN 1109-2734.
- [JR.6] With P. Di Felice, "A System-Level HW/SW Co-Design Methodology for Ad-Hoc Implementation of DBMS Operators", *WSEAS TRANSACTIONS on COMPUTER RESEARCH*, Issue 2, Volume 2, February 2007 ISSN 1991-8755.
- [JR.7] With P. Di Felice, M. Ianni. "Design and evaluation of a spatial extension of TinyDB for wireless sensor networks", *International Journal of Computers and Their Applications Manuscript*, to appear in September 2010 issue.

THESIS

- [TH.1] (Italian) "La qualità dei dispositivi con proprietà di autodiagnosi: una metodologia di valutazione innovativa", Tesi di Laurea, Politecnico di Milano - DEI, Milano 1998.
- [TH.2] (Italian) "Co-Simulazione HW/SW a livello di sistema", Tesi di Master, XI^o Master IT, Centro CEFRIEL, Milano 1999.
- [TH.3] "System-Level Co-Design of Heterogeneous Multiprocessor Embedded Systems", Tesi di Dottorato, Politecnico di Milano – DEI, Milano 2002.

TECHNICAL REPORTS

- [RP.1] "An overview of parallel-embedded architectures for real-time applications", *Rapporto Interno No. 2000.25*, Politecnico di Milano – DEI, Milano 2000.
- [RP.2] "System Level Concurrent Error Detection", *Rapporto Interno No. 2001.62*, Politecnico di Milano – DEI, Milano 2001.
- [RP.3] with W. Fornaciari. "SystemC+: Generic Class Library User Guide", *IST Project N. 1999-11476 - Odette*, <http://odette.offis.de/>.
- [RP.4] with P. Di Felice, "Integration of spatial data types and operators into relational DBMSs: a survey", *Rapporto Interno R.06-84*, Università dell'Aquila-DIEI, 2006.
- [RP.5] with P. Di Felice, Carlo Brandolese, Daniele Scarpazza, "Parsing SystemC: an open-source, easy to extend parser", *Rapporto Interno R.06-85*, Università dell'Aquila, 2006.