PROJECTS/THESIS 11/2017

C4uC
(please contact marco.santic@univaq.it and walter.tiberti@graduate.univaq.it)

WIP

WIRELESS SENSOR NETWORKS
(please contact marco.santic@univaq.it and walter.tiberti@graduate.univaq.it)

1) Analysis and experimentation of OSs and protocol stacks for WSN
2) Analysis and experimentation/development of agent-based middleware for WSN
3) Analysis and experimentation/development of advanced algorithms for WSN-based localization and indoor tracking
4) LabSMILING
   a) Enhancement of a remote lab/testbed for WSN
   b) Analysis and experimentation of JTAG interface and debugging on WSN motes platforms
   c) Development of a 3D representation of IEEE 802.15.4 radio signal in indoor and outdoor spaces
   d) Enhancement of the platform for the Wireless Sensor NetWars Competition
5) WSN Security
   a) Interfacing of FPGA and sensor nodes for HW acceleration of ECC algorithms
   b) Analysis and experimentation of novel WSN-oriented cryptography algorithms
   c) Analysis and experimentation of microcontroller-oriented memory-dumping techniques
   d) Analysis of TAKS scheme and development of targeted attacks and countermeasures
   e) Analysis and experimentation of “Row hammer” attack on WSN motes
   f) Analysis of heap implementation on WSN motes and experimentation of “heap overflow” attacks
   g) Analysis and experimentation of “Power Analysis” attack techniques targeting WSN motes
   h) Analysis and replication of a WSN mote HW model and simulator
   i) Analysis and experimentation of WSN-oriented secure hash and MAC functions
   j) Analysis and experimentation of WSN intrusion attacks
   k) Analysis and experimentation of security features of microcontroller TI CC2538

REAL-TIME SYSTEMS
(please contact giacomo.valente@graduate.univaq.it and vittoriano.muttillo@graduate.univaq.it)

1) Analysis of RTOS on embedded platform
   a) VxWorks
   b) FreeRTOS
   c) Linux Related Real-Time Kernels
      i) RTLinux, RTAI, and Xenomai
      ii) PREEMPT RT, SCHED EDF, and Linux/RK projects
   d) RTEMS
   e) Erika Enterprise, an OSEK kernel for small embedded platform
   f) Shark, a POSIX-like kernel for PC platforms
   g) Marte OS, a POSIX-like kernel for PC platforms supporting C++ and Ada 2005
   h) MQX
   i) FINX operating systems in collaboration with MBDA Finmeccanica/Leonardo
   j) ThreadX
   k) Nucleus
   l) eCos
2) Benchmarking of RTOS on ARM, LEON3, Microblaze and NiosII processors
3) Analysis of LITMUS (Linux Testbed for Multiprocessor Scheduling in Real-Time Systems, http://www.litmus-rt.org/), a Linux kernel extension that allows to test real-time operating systems.

4) Testing MAST (Modeling and Analysis Suite for Real-Time Applications, http://mast.unican.es/), an open-source suite of tools to perform schedulability analysis of real-time systems.

MULTI/MANY-CORE SYSTEMS
(please contact giacomo.valente@graduate.univaq.it)

1) Development of a monitoring system for multi-core scenario on FPGA, able to work with Rapitime tool (https://www.rapitasystems.com/products/rapitime) without inserting software overhead.
2) Development of monitoring system for multi-core scenario on FPGA able to communicate its results using a DMA controller.
3) Program an Asymmetric Multi-Processing platform that is composed of 6 heterogeneous processors. The application is an indoor localization algorithm that is computationally heavy, so it needs a multi-core architecture to work faster.
4) Implementation of runtime partial reconfiguration on Zynq7000 device, and create a system that is adaptive with respect to the scenario where it will work. Analysis of advantages of partial dynamic reconfiguration action.
5) Development of a software layer able to interface perfmon2 to a custom hardware profiling system for soft-processors.
6) Porting of BARBEQUE open source system (http://bosp.dei.polimi.it/) on LEON3+Linux/based multi-processor platform on FPGA.
8) Test a RISC-V based architecture on Zynq7000 SoC.

PARALLEL PROGRAMMING MODELS
(please contact giacomo.valente@graduate.univaq.it and vittoriano.muttillo@graduate.univaq.it)

1) Analysis and experimentation of parallel programming libraries through experimentation on a few specific architectures (MicroBlaze, LEON3, arm, x86, etc.):
   a) OpenMPI: https://www.open-mpi.org/
   b) OpenMP: http://openmp.org/wp/
   c) OpenCL: https://www.khronos.org/opencl/ MCAPI: http://www.multicore-association.org/workgroup/mcapi.php
   d) OpenAMP: http://www.multicore-association.org/workgroup/oamp.php

MIXED-CRITICAL SYSTEMS
(please contact vittoriano.muttillo@graduate.univaq.it)

1) Analysis and experimentation of HYPERVISORS (Xtratum, PikeOS, XEN): drivers development and performances comparison.
2) Analysis and development of Mixed-Criticality Network-On-Chip.

HW/SW CO-DESIGN
(please contact vittoriano.muttillo@graduate.univaq.it)

1) Analysis and experimentation of methodologies and IDE for HW/SW co-design
2) Analysis and experimentation/development of C/C++/SystemC-based HW/SW co-simulators
   a) Development of tool for automatic instrumentation of SystemC code
   b) Analysis and experimentation of WINDRIVER SIMICS (Virtual Platforms Simulator)
   c) Analysis and experimentation/extension of Intel CoFluent
3) Analysis and experimentation/development of SW tools for evaluation/analysis of SystemC metrics and simulation:
   a) Timing: CC4CS (HW)

   b) Size: S4CS (HW/SW)
   c) Power/Energy: J4CS (HW/SW)
   d) Timing Simulation
4) Analysis and experimentation/development of tools for Design Space Exploration
   a) Extension of PAM1
   b) PAM2

TOOLS/KITS ANALYSIS AND TESTING
(please contact giacomo.valente@graduate.univaq.it and vittoriano.muttillo@graduate.univaq.it)

1) Parallel Programming Analysis and tools
   a) Aftermath (https://www.aftermath-tracing.com/)
   b) DASH (http://www.dash-project.org/home.html)
2) HW/SW Co-Design
   a) PREESM + SPIDER + PAPIfy
   b) eSSYN (Embedded software synthesis) + Contrep + VIPPE (http://essyn.com/, http://umlmarte.teisa.unican.es/index.php/documentation/)
   c) ForSyDE (https://forsyde.ict.kth.se/trac)
   d) Gezel (http://rijndael.ece.vt.edu/gezel2/)
3) High-Level Synthesis Tools
   a) CAPH HLS (http://caph.univ-bpclermont.fr/CAPH/CAPH.html)
   b) LegUP HLS (http://legup.eecg.utoronto.ca/)
   c) PandA project and Bambu HLS (https://panda.dei.polimi.it/)
4) Run-Time Reconfiguration
   a) ARTICO^3 (Universidad Politécnica de Madrid)
   b) FRED Framework Analysis (Scuola Superiore Sant'Anna di Pisa)
5) Others
   a) MIPSfpga (https://community.imgtec.com/iup_events/mipsfpga-half-day-workshop-at-d-a-t-e-2016/)
   b) Xilinx University Program System Design on Zynq using SDSoC (https://www.xilinx.com/products/design-tools/software-zone/sdsoc.html)
   c) Analysis and experimentation of radCASE+radCHECK (http://www.radcase-ux.com/en/index.php)

OTHER
(please contact giacomo.valente@graduate.univaq.it, vittoriano.muttillo@graduate.univaq.it and luigi.pomante@univaq.it)

1) Improve digital camera example with a new 8051 HDL model
2) Analysis and experimentation of Biometric Badge
3) Analysis and experimentation of LEGO Mindstorm EV3 (https://www.lego.com/it-it/mindstorms/products/mindstorms-ev3-31313)
4) Analysis and experimentation of TULIPP platform (http://tulipp.eu/)
5) Thesis in Skytechnology Srl (http://www.skytechnology.it/en/)
   a) Porting of VxWorks to a legacy board
   b) Analysis and experimentation of a legacy IP TOE-FX101 (TCP-IP core engine) on FPGA (es. PCIe linux driver)