Thesis/Project proposal

Name	System-Level Design Space Exploration for Heterogeneous Parallel Dedicated Real-Time Systems
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Type	Implementation, Research
Keywords	EDA, DSE, Real-Time
Description	The work focuses on the extension of an ESL HW/SW Co-Design methodology in order to consider also real-time constraints. In particular, the goal is to improve an existing DSE approach to suggest implementations that are able to satisfy different kind of timing constraints: - Time to Completion - Time to Reaction - Extended Time to Reaction
Expected Duration	2-3 months
References (Online)	L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. “Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC”, IEEE Transactions on Computers, vol. 55, no. 5, May 2006. L. Pomante, “System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems”. IEEE International Conference on Application-specific Systems, Architectures and Processors, Santa Monica, Settembre 2011. V. Muttillo, G. Valente, D. Ciambrone, V. Stoico, and L. Pomante, “HEPSYCODE-RT: a Real-Time Extension for an ESL HW/SW Co-Design Methodology”, Proceedings of the 10th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO’18), ACM, New York, NY, USA, 2018, https://dl.acm.org/citation.cfm?id=3180670. L. Pomante, G. Valente, V. Muttillo, D. Ciambrone. “HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems”, In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS’2018), Budva, Montenegro, 2018.
References (Attached)	