Thesis/Project proposal

Name	CC4CS/JC4CS Performance Metrics
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Type	Implementation, Research
Keywords	Performance Analysis, HW/SW Co-Design, Instruction Set Simulators, Python, Descriptive Statistics
Description	The thesis focuses on the evaluation and the analysis of a performance metric for HW/SW technologies, called CC4CS (*Clock Cycles for C Statement*), for early-stage performance estimation. The values of CC4CS are obtained by executing a C benchmark by means of both ISS (for GPP/ASP) and HLS/HDL environments (for SPP). The evaluation process is automated thanks to a Python-based framework. The first part of the work regards the maintenance and the improvement of the framework as well as the evaluation of CC4CS values for several processors. In the second part, the obtained values are analyzed to carry on the performance estimation, compare the involved processors, and analyze estimation errors [1]. Further evolutions of the work are related to energy/power consumption estimations based on the same framework (J4CS - *Joule for C Statement*).
Expected Duration	3-4 months
References (Online)	[1] https://dl.acm.org/citation.cfm?doid=3185768.3186291
References (Attached)	