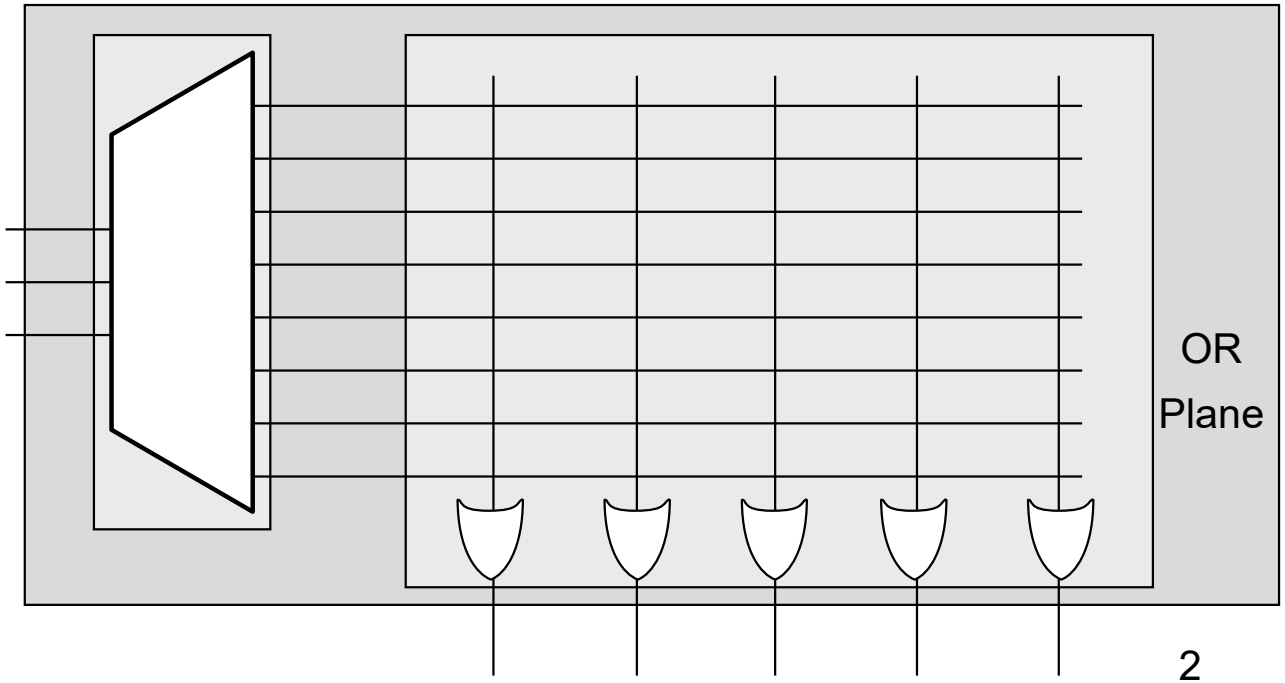
Embedded Systems

IC Technologies
Exercises

2-Levels PLD

- Read-Only Memory (ROM/PROM)
  - Ex ROM-1
    - Is it possible to use the ROM in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the ROM accordingly.

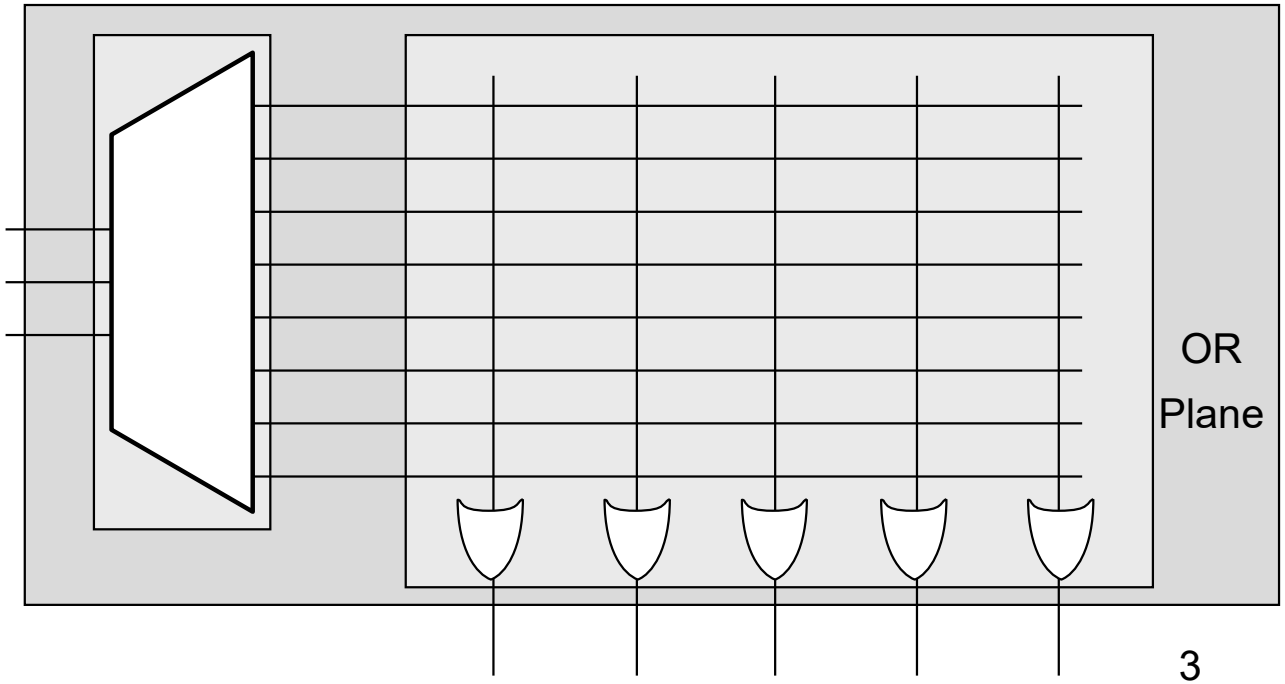
abc	f_1	f_2	f_3	f_4	f_5
000	1	0	0	1	1
001	1	1	1	1	1
010	0	0	1	0	1
011	1	1	1	1	0
100	1	1	1	1	1
101	1	1	1	1	1
110	1	0	0	1	1
111	1	1	0	1	1



2-Levels PLD

- Read-Only Memory (ROM/PROM)
  - Ex ROM-2
    - Is it possible to use the ROM in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the ROM accordingly.

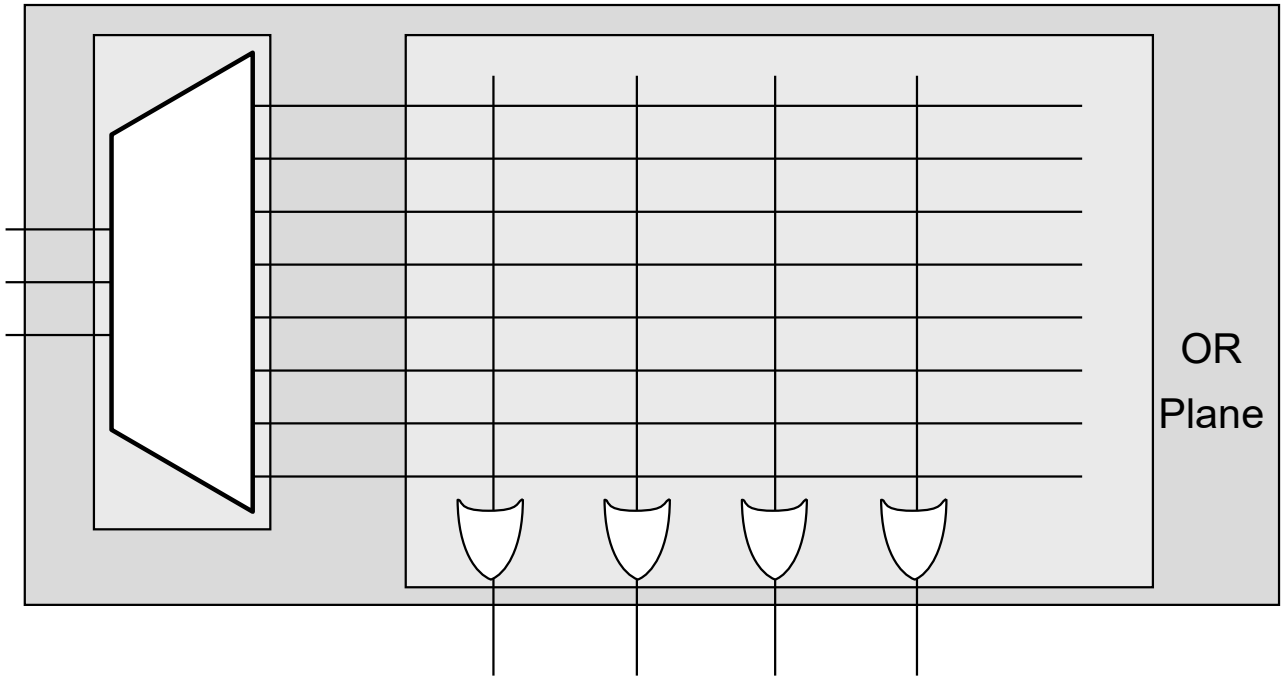
abc	f_1	f_2	f_3
000	0	0	0
010	0	0	1
011	1	1	1
100	1	1	1
101	1	1	1



2-Levels PLD

- Read-Only Memory (ROM/PROM)
  - Ex ROM-3
    - Is it possible to use the ROM in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the ROM accordingly.

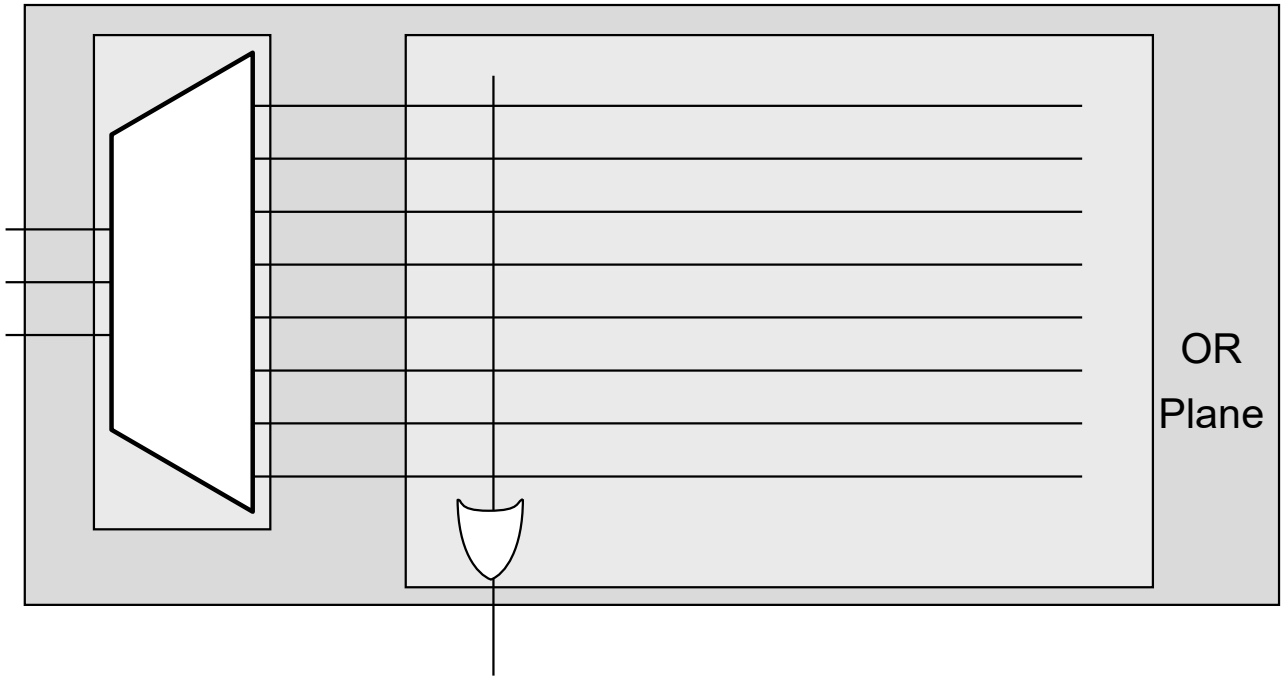
abc	f_1	f_2	f_3	f_4	f_5
000	1	0	0	1	1
001	1	1	1	1	1
010	0	0	1	0	1
011	1	1	1	1	0
100	1	1	1	1	1
101	1	1	1	1	1
110	1	0	0	1	1
111	1	1	0	1	1



2-Levels PLD

- Read-Only Memory (ROM/PROM)
  - Ex ROM-4
    - Is it possible to use the ROM in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the ROM accordingly.

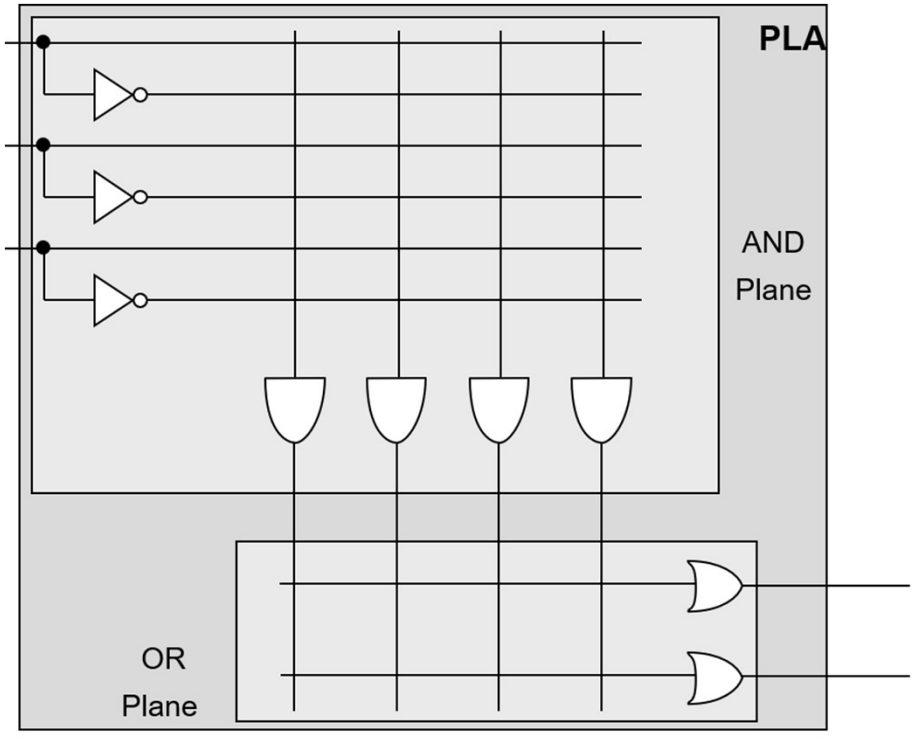
ab	f_1
00	1
01	0
10	1
11	1



2-Levels PLD

- Programmable Logic Array (PLA)
  - Ex PLA-1
    - Is it possible to use the PLA in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the PLA accordingly.

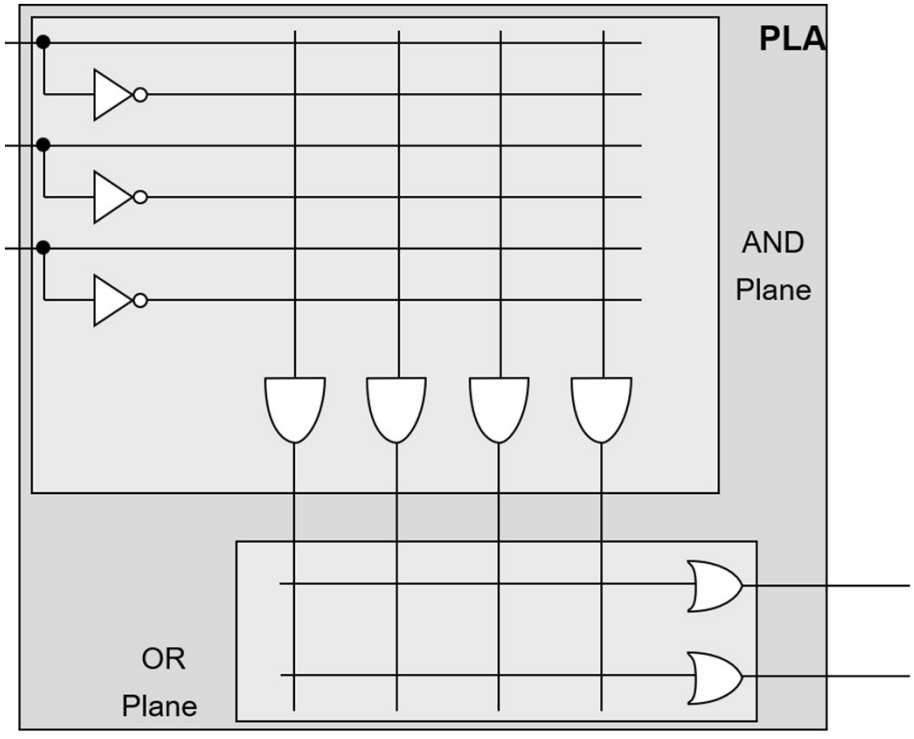
ab	f_1
00	1
01	0
10	1
11	1



2-Levels PLD

- Programmable Logic Array (PLA)
  - Ex PLA-2
    - Is it possible to use the PLA in the figure to implement the combinatorial network specified by the true table below?
      - If yes, "program" the PLA accordingly.

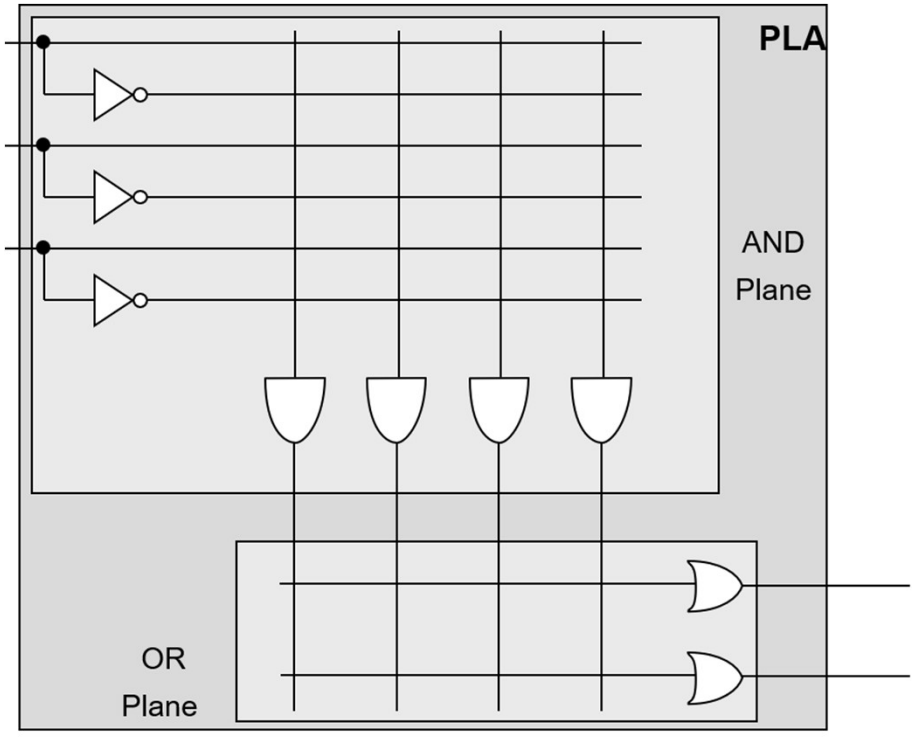
abc	f_1	f_2	f_3
000	0	0	0
010	0	0	1
011	1	1	1
100	1	1	1
101	1	1	1



2-Levels PLD

- Programmable Logic Array (PLA)
  - Ex PLA-3
    - Is it possible to use the PLA in the figure to implement the combinatorial network specified by the logic equations below?
      - If yes, "program" the PLA accordingly.

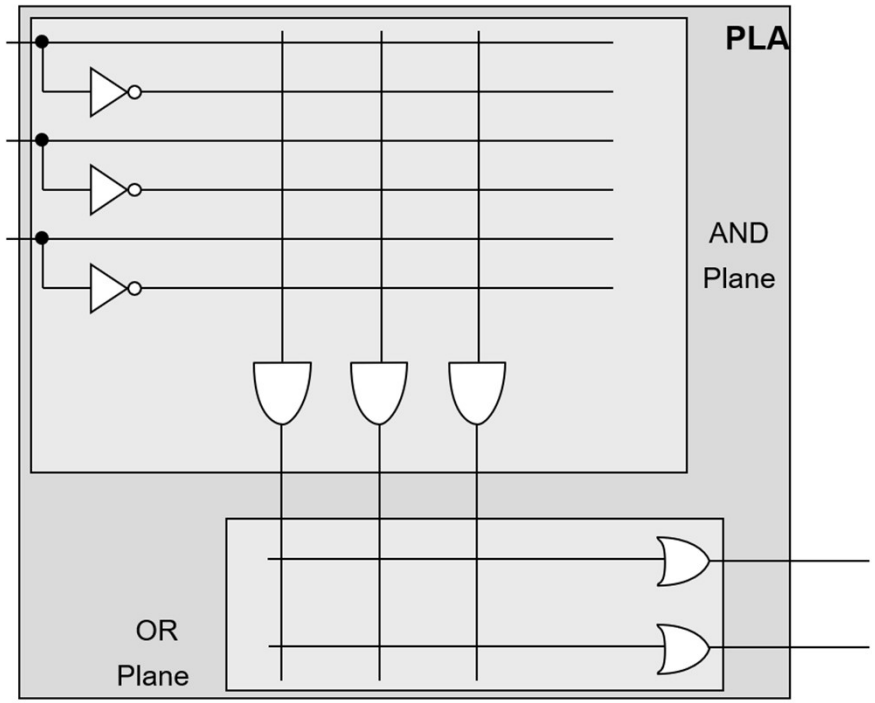
f1 = ab + ac'+ b'c
f2 = ab + a'c + b'c



2-Levels PLD

- Programmable Logic Array (PLA)
  - Ex PLA-4
    - Is it possible to use the PLA in the figure to implement the combinatorial network specified by the logic equations below?
      - If yes, "program" the PLA accordingly.
        - » Are really needed two output lines from tre OR plane?

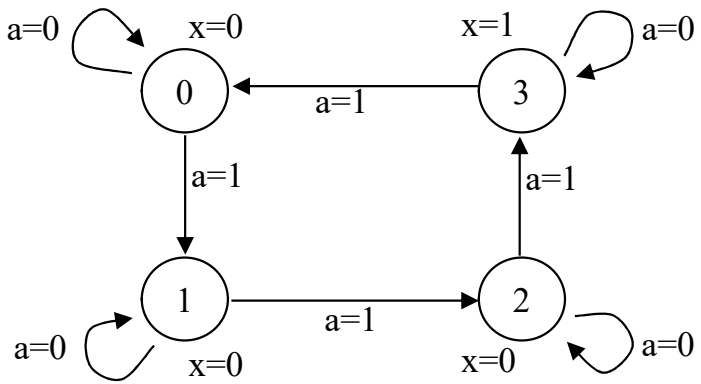
f1 = a + ac’
f2 = ab + a + ac’



Multi-level PLD

- Advanced PLA
  - Ex APLA-1
    - Is it possible to use the Advanced PLA in the next slide to implement the sequential network specified by the state diagram below?
      - If yes, "program" the Advanced PLA accordingly.

State Diagram

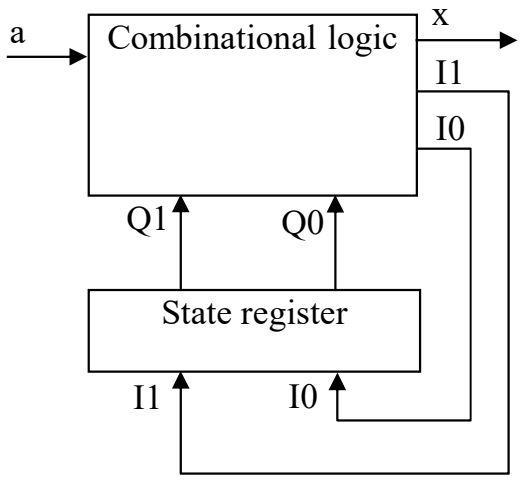


State Table (Moore-type)

Inputs			Outputs		
Q1	Q0	a	I1	I0	x
0	0	0	0	0	0
0	0	1	0	1	
0	1	0	0	1	0
0	1	1	1	0	
1	0	0	1	0	0
1	0	1	1	1	
1	1	0	1	1	1
1	1	1	0	0	

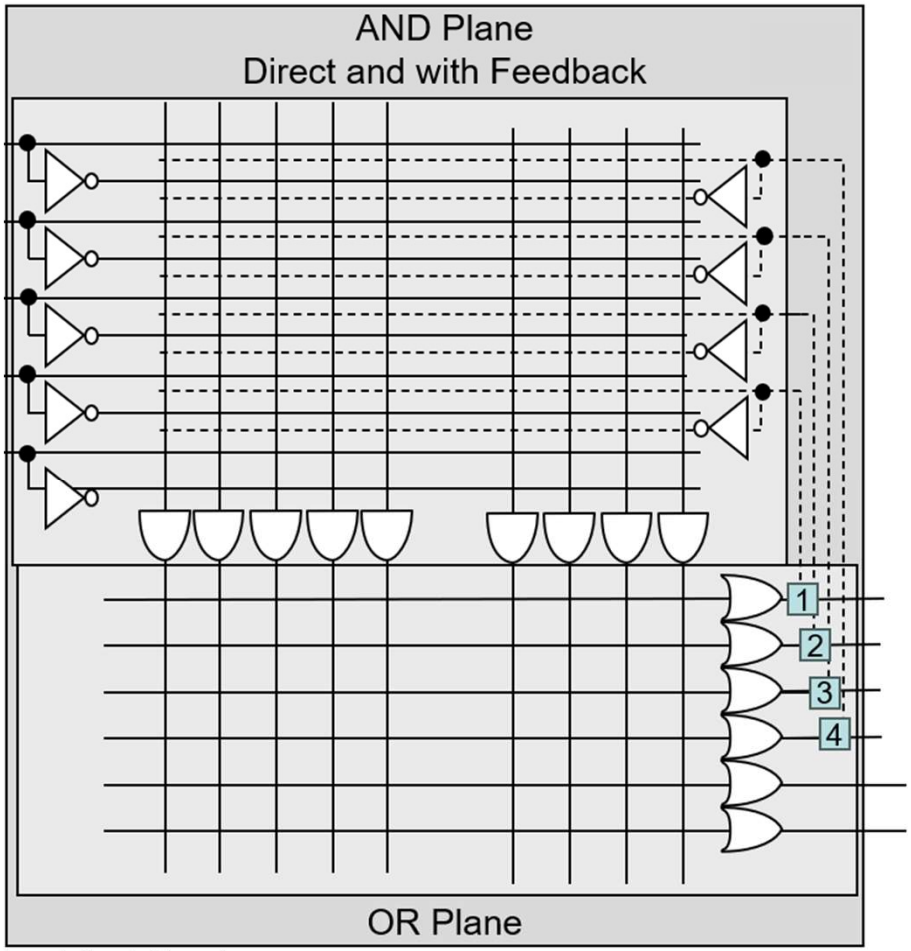
I1 = Q1'Q0a + Q1a' + Q1Q0'
I0 = Q0a' + Q0'a
x = Q1Q0

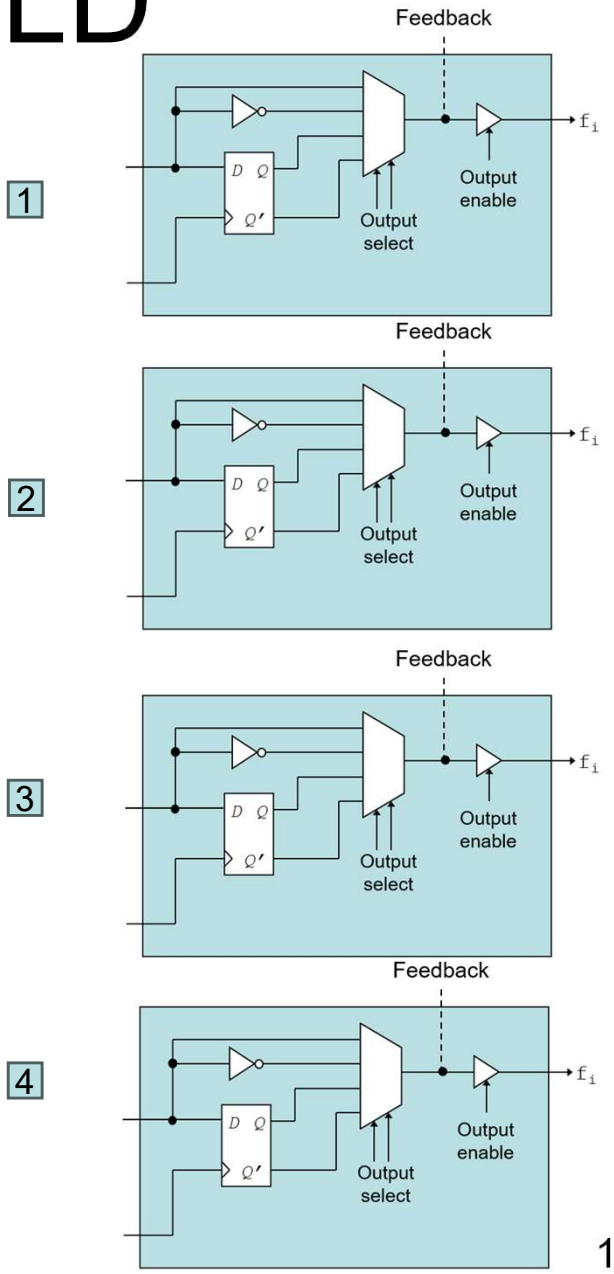
Implementation Model



Multi-level PLD

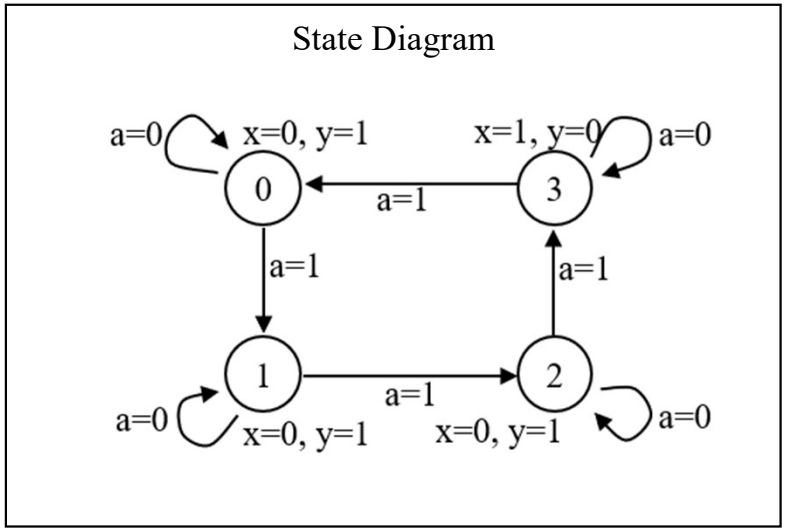
- Advanced PLA/PAL
  - Ex APLA-1





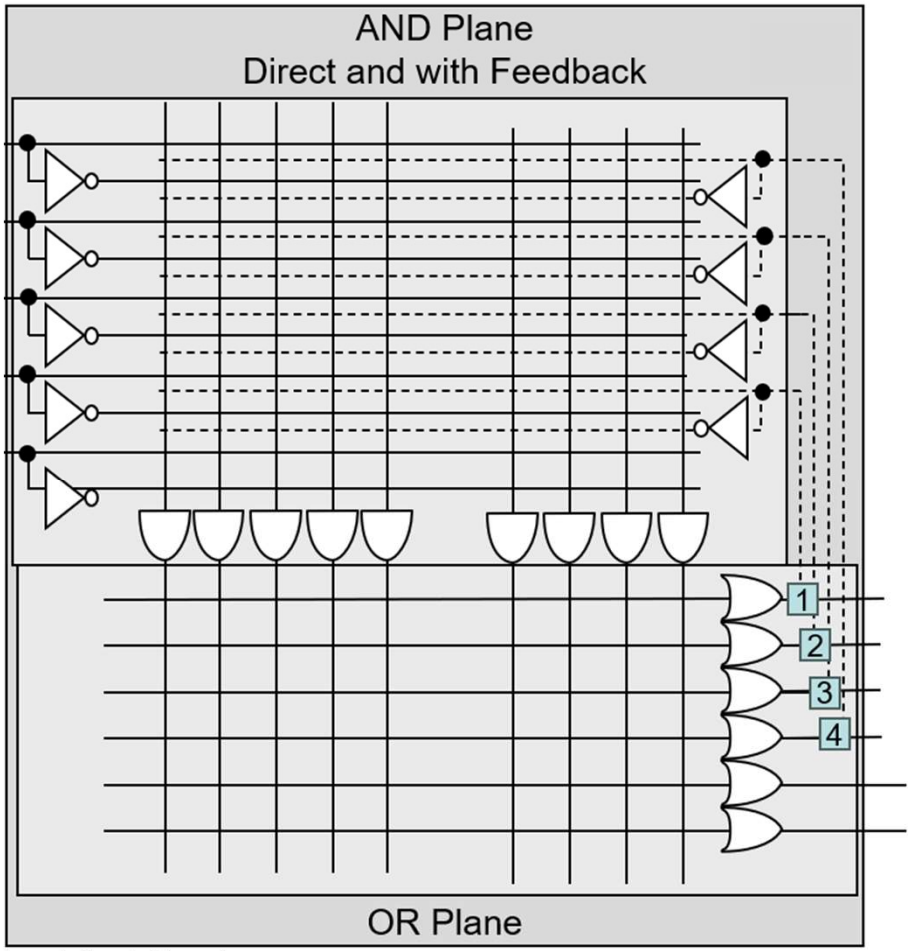
Multi-level PLD

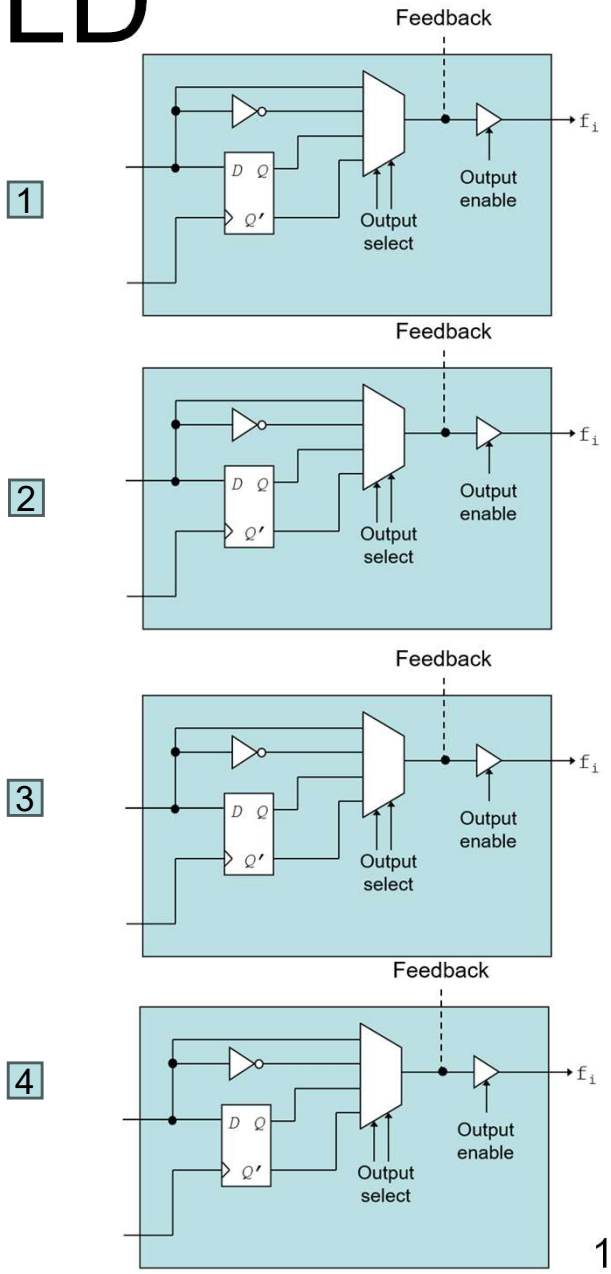
- Advanced PLA
  - Ex APLA-2
    - Is it possible to use the Advanced PLA in the next slide to implement the sequential network specified by the state diagram below?
      - If yes, "program" the Advanced PLA accordingly.



Multi-level PLD

- Advanced PLA/PAL
  - Ex APLA-2





Multi-level PLD

- Advanced PLA
  - Ex APLA-3
    - With reference to the Advanced PLA shown in the next slide, what is the general relation between the number of outputs and the number of states that can be represented?
      - Is it possibe to identify some exceptions (i.e., special cases) to the general rule?

Multi-level PLD

- Advanced PLA/PAL
  - Ex APLA-3

