Università degli Studi dell'Aquila

Center of Excellence DEWS

DESIGN SPACE EXPLORATION FOR DEDICATED DIGITAL ELCTRONIC SYSTEMS

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Overview

HW/SW CODESIGN

It is an HW/SW concurrent design methodology that allows to keep a unified and technology independent vision of the developed digital electronic system

Starting Point

Dr. Luigi Pomante

"HW/SW Co-Design of Dedicated Heterogeneous Parallel Systems: an Extended Design Space Exploration Approach". IET Computers & Digital Techniques, Institution of Engineering and Technology, 2013, Vol. 7, Iss. 6, pp. 246–254.

Eng. Paolo Serri

"Esplorazione dello spazio di progetto
per sistemi embedded multi-processore"
Master Thesis – Computer Science Engineering –2013

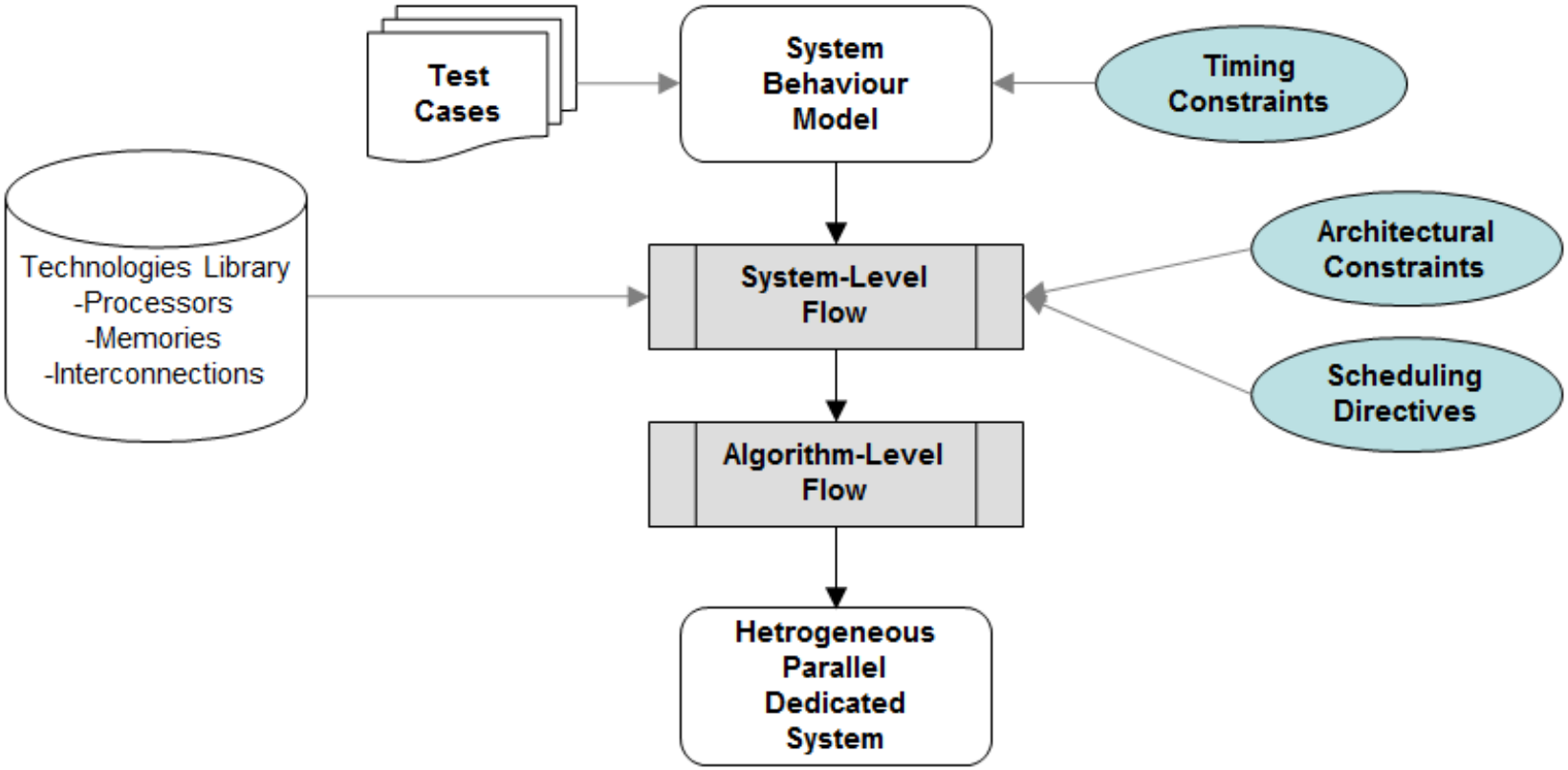
Goals

1) Starting point analysis
   - HW/SW co-design flow
   - DSE tool architecture

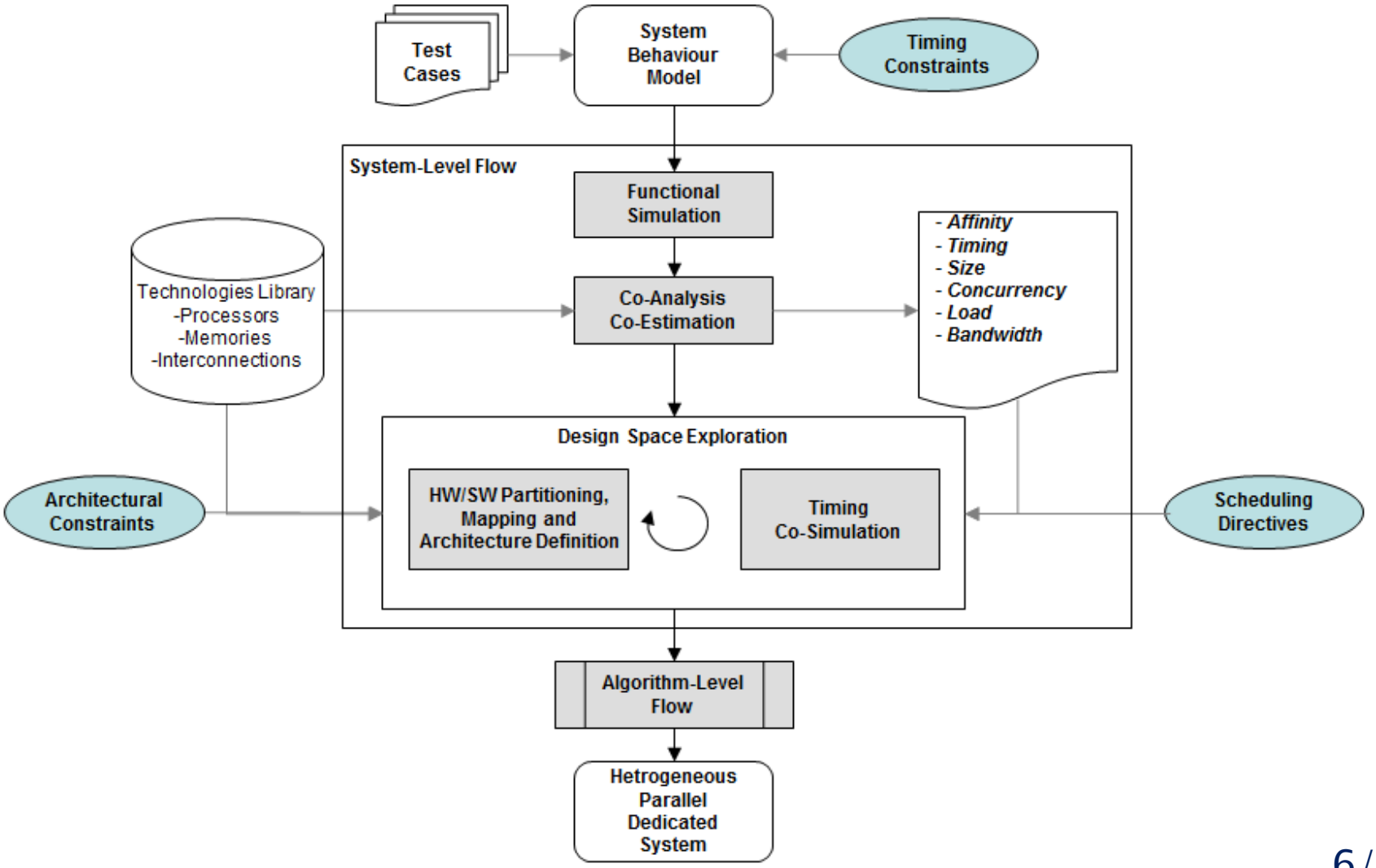
2) Extensions and improvements

3) V&V

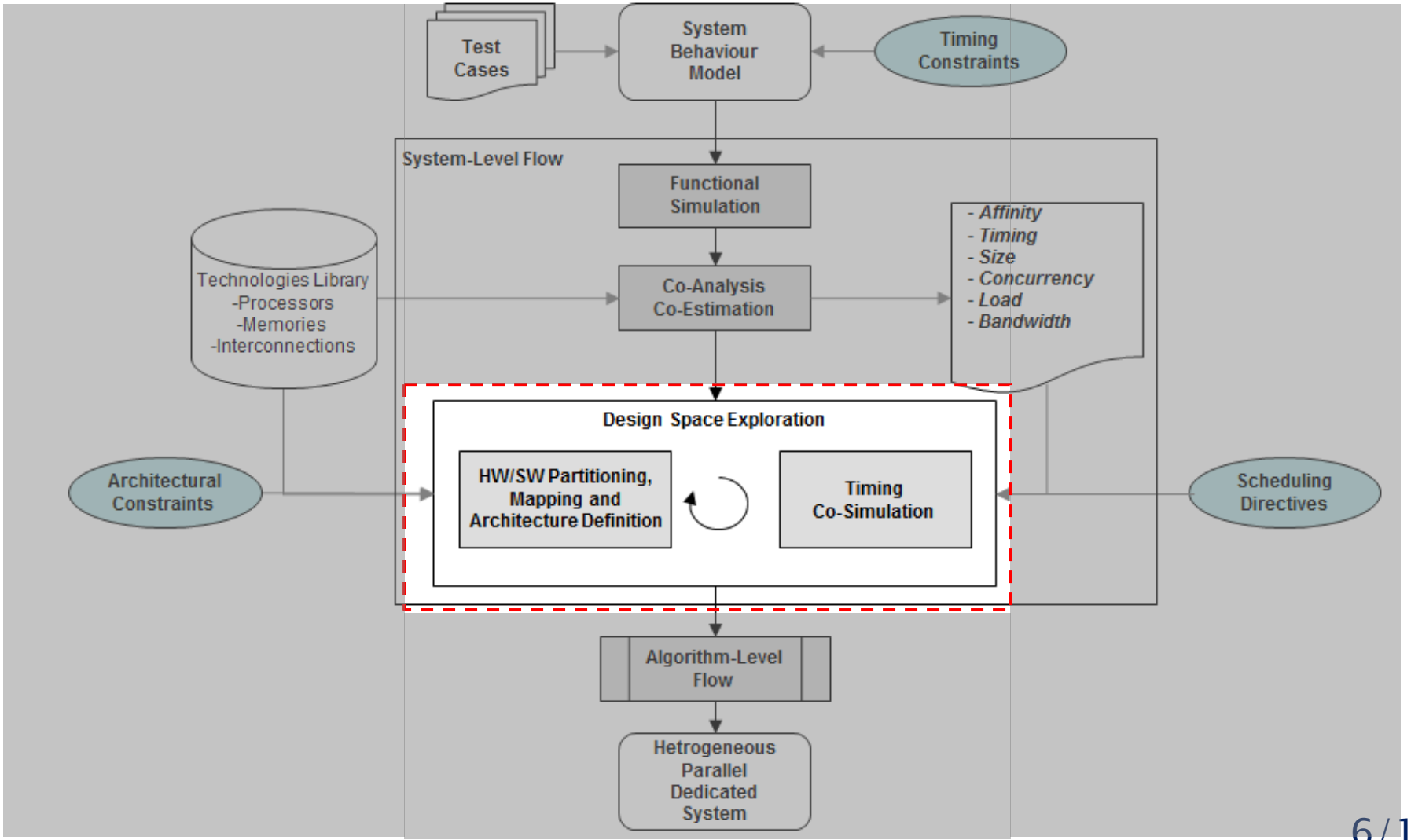
HW/SW co-design flow



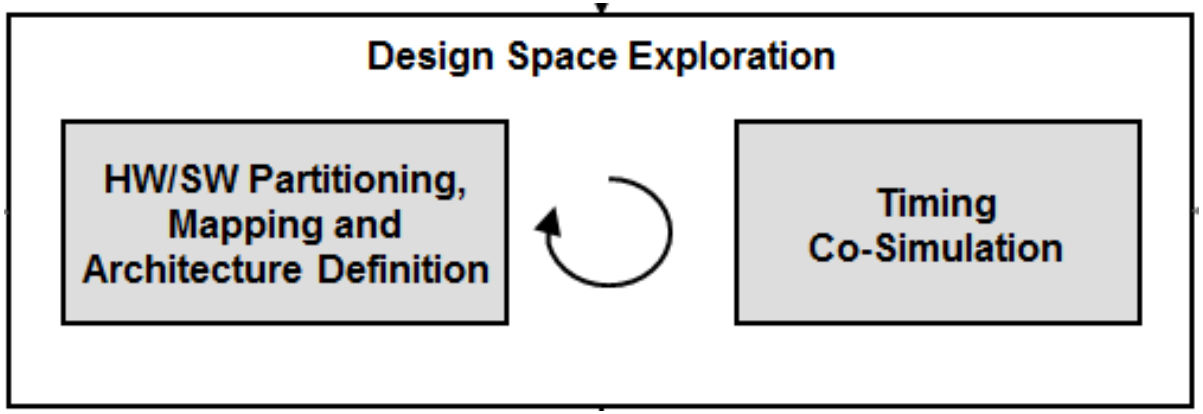
HW/SW co-design flow



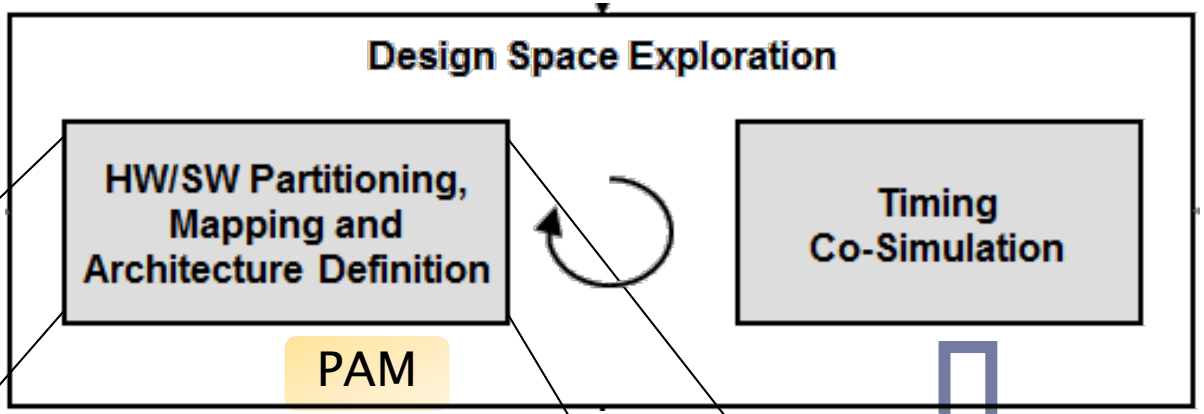
HW/SW co-design flow: DSE



HW/SW co-design flow: DSE



HW/SW co-design flow: DSE



PAM1

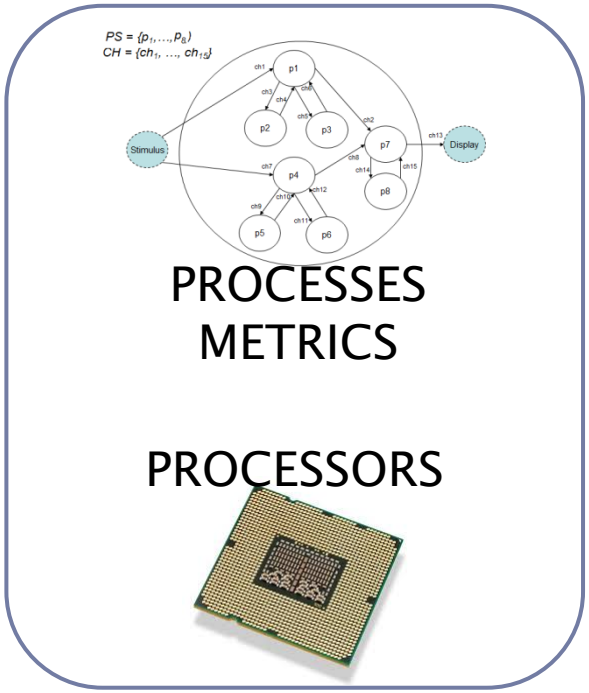
- HW/SW partitioning
- How many and which processors
- Mapping

PAM2

- Processors interconnection

Timing constraints verifcation

DSE Tool Architecture



Extensions and improvements

Key point of the work has been to adapt PAM1 tool to manage new input data to allow the exploration of a more complex design space

It is now possible to consider more processors types (GPP, DSP, SPP) and processors models (e.g. GPP Intel MPU8051, DSP Microchip PIC24, SPP Xilinx SPARTAN3AN,…)

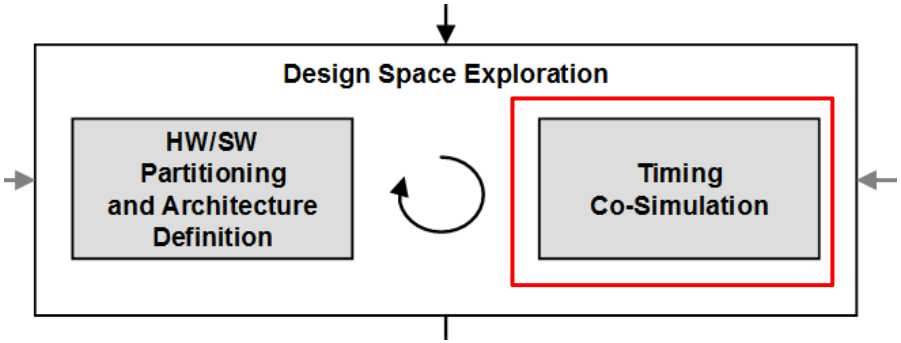
V&V

VERIFICATION

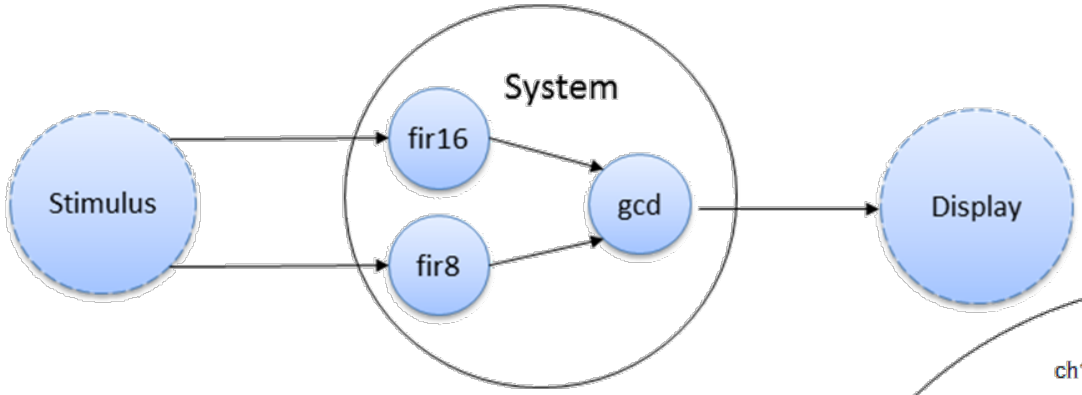
Simple use cases and manual check of the results

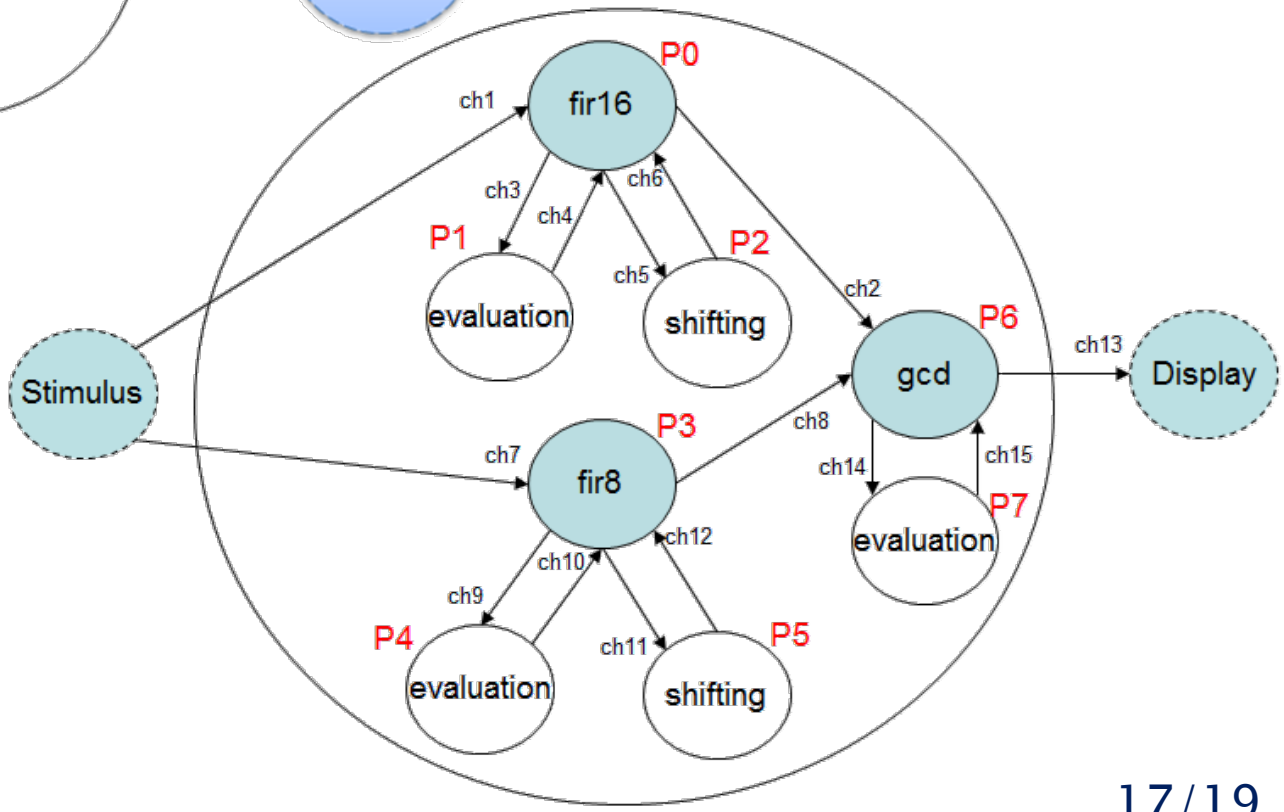
VALIDATION

More complex use case and partial application of a SystemC-based co-design flow



V&V: use case

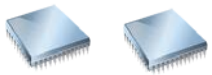




Processors

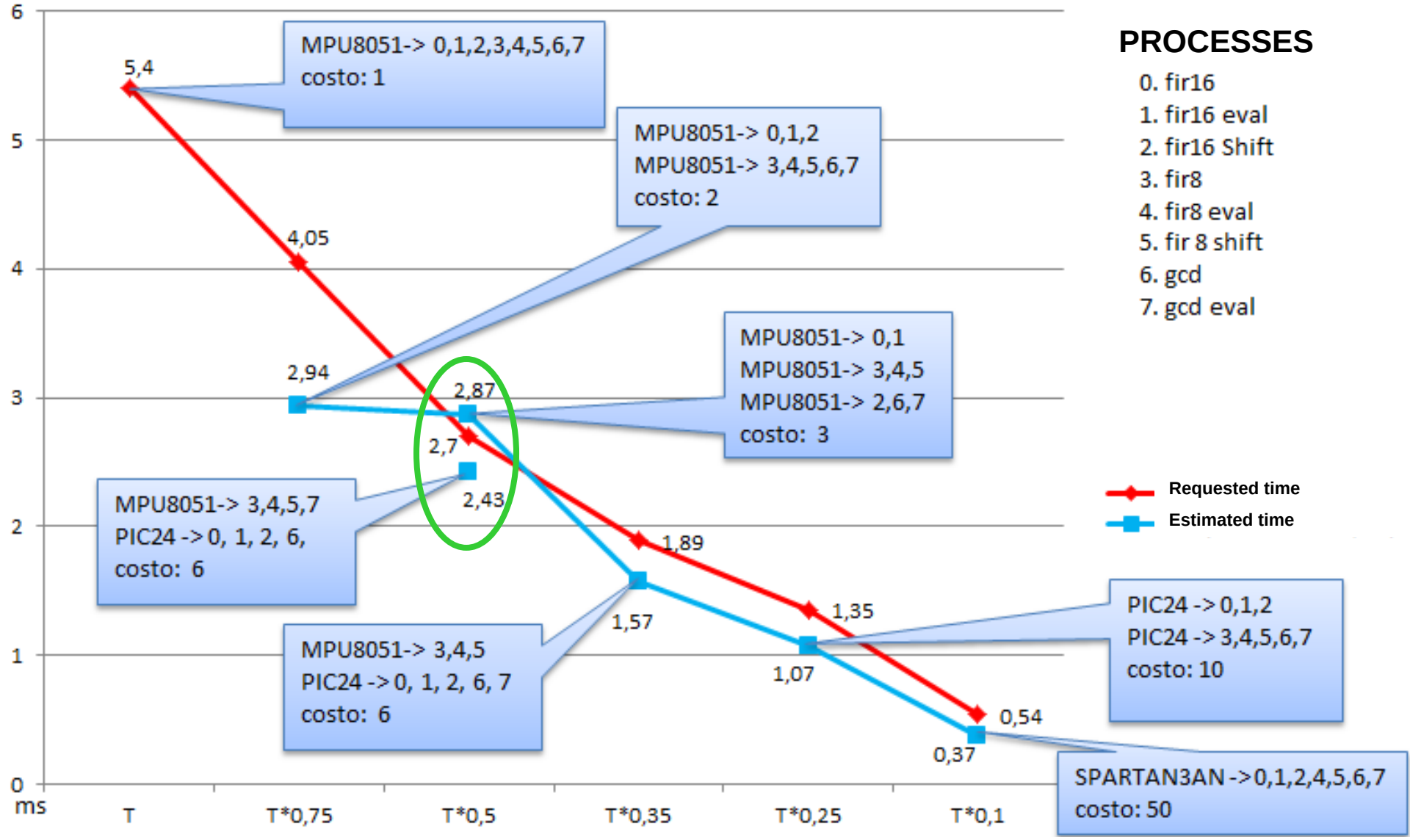
Intel MPU8051

Microchip DSPIC (Pic24)



Xilinx Spartan3AN

V&V: results


6
5
4
3
2
1
0
ms
T
T*0,75
T*0,5
T*0,35
T*0,25
T*0,1
5,4
4,05
2,94
2,87
2,7
2,43
1,89
1,57
1,35
1,07
0,54
0,37
MPU8051-> 0,1,2,3,4,5,6,7
costo: 1
MPU8051-> 0,1,2
MPU8051-> 3,4,5,6,7
costo: 2
MPU8051-> 0,1
MPU8051-> 3,4,5
MPU8051-> 2,6,7
costo: 3
MPU8051-> 3,4,5,7
PIC24 -> 0, 1, 2, 6,
costo: 6
MPU8051-> 3,4,5
PIC24 -> 0, 1, 2, 6, 7
costo: 6
PIC24 -> 0,1,2
PIC24 -> 3,4,5,6,7
costo: 10
SPARTAN3AN -> 0,1,2,4,5,6,7
costo: 50
PROCESSES
0. fir16
1. fir16 eval
2. fir16 Shift
3. fir8
4. fir8 eval
5. fir 8 shift
6. gcd
7. gcd eval
Requested time
Estimated time

Conclusions

- Thanks to the flexible design of the existing DSE-PAM1 tool it has been possible to improve the tool with a mimimal effort
- Positive validation results (by means of HW/SW timing co-simulation)
- Conference publication
  - Pomante, Serri, Incerto, Volpe. “HW/SW Co-Design of Heterogeneous Multiprocessor Dedicated Systems: a SystemC-based Environment”. 2th World Congress on Modelling, Analysis and Simulation of Computer Systems 2014 (ICTMASCS'2014)

FUTURE WORKS

PAM2 Implementation & Intel CoFluent integration

Genetic algorithm multi-thread implementation

Validation by means of real platform