Electronic System-Level HW/SW Co-Design

C/C++/SystemC and/or UML/MARTE/UPPAAL for the development of methodologies and related tool chains.

ID	01
Title	Trace analyzer for HW/SW co-simulations
Contacts	Luigi Pomante (luigi.pomante@univaq.it)
Description	The work aims at developing a tool to visualize and analyze traces (in CTF and/or VCD format) that shall be extracted during HW/SW co-simulations based on HEPSIM (i.e., the HW/SW co-simulator used in HEPSYCODE).
References	CTF: https://diamon.org/ctf/ VCD: https://en.wikipedia.org/wiki/Value_change_dump HEPSIM: D. Ciambrone, V. Muttillo, L. Pomante, G. Valente. "HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems", In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS'2018), 2018.

ID	02
Title	Affinity metric and tool
Contacts	Luigi Pomante <luigi.pomante@univaq.it> Vittoriano Muttillo <vittoriano.muttillo@univaq.it>
Description	The work focuses on the extension of a system-level metric for HW/SW technologies, called *Affinity*. The goals are: - to improve the metric to better consider GPP/DSP/SPP (also analyzing SoA) - to extend the metric to consider also GPUs and/or other technologies - to develop a tool for the (semi)automatic evaluation of the metric (possibly considering also Machine Learning approaches)
References	[1] L. Pomante, W. Fornaciari, F. Salice, D. Sciuto. "Metrics for Design Space Exploration of Heterogeneous Multiprocessor Embedded System", *IEEE/ACM International Workshop on Hardware Software Co-Design* (IEEE/ACM CODES 2002), Colorado (USA), Maggio 2002.

	[2] L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC", IEEE Transactions on Computers, vol. 55, no. 5, Maggio 2006.

ID	03
Title	CC4CS/J4CS Metrics and tools
Contacts	Luigi Pomante <luigi.pomante@univaq.it> Vittoriano Muttillo <vittoriano.muttillo@univaq.it> Vincenzo Stoico <vincenzo.stoico@student.univaq.it>
Description	The work focuses on the evaluation and the analysis of timing/energy metrics for HW/SW technologies, called CC4CS (*Clock Cycles for C Statement*) and J4CS (*Joule for C Statement*) for early-stage performance estimation. The goals are: - to improve the metrics using the intermediate representations (IR) of the compiler (GCC, LLVM). - to evaluate and analyze the metrics for new processors (e.g., ARM, Microblaze, etc.) - to extend the metrics to consider also issues related to "size" (e.g., byte for C statement and/or FPGA-resources for C statement)
References	[1] V. Muttillo, G. Valente, L. Pomante, V. Stoico, F. D'Antonio, and F. Salice, "CC4CS: an Off-the-Shelf Unifying Statement-Level Performance Metric for HW/SW Technologies", In Companion of the 2018 ACM/SPEC International Conference on Performance Engineering (ICPE '18), ACM, 2018, pp. 119-122. [2] V. Muttillo, P. Giammatteo, V. Stoico, L. Pomante. An Early-Stage Statement-Level Metric for Energy Characterization of Embedded Processors. Microprocessors and Microsystems, 2020. [3] https://llvm.org/devmtg/2017-06/1-Davis-Chisnall-LLVM-2017.pdf

ID	04
Title	System-Level Design Space Exploration for Approximate Dedicated Computing Systems
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)

Description	The work focuses on the extension of an ESL HW/SW Co-Design methodology (i.e., HEPSYCODE) to consider Approximate Computing techniques. In particular, the goals are to improve an existing *Design Space Exploration* approach to suggest implementations that: - exploit existing approximate computing techniques (that needs to be analyzed, classified and characterized) to satisfy accuracy, energy and timing requirements
References	[1] L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC", IEEE Transactions on Computers, vol. 55, no. 5, May 2006. [2] L. Pomante, "System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems". IEEE International Conference on Application-specific Systems, Architectures and Processors, Santa Monica, Settembre 2011. [3] L. Pomante, P. Serri. "SystemC-based HW/SW Co-Design of Heterogeneous Multiprocessor Dedicated Systems". International Journal of Information Systems, Journal ISSN Online: 2356-5896, Vol. 1, July 2014. [4] Luigi Pomante, Vittoriano Muttillo, Marco Santic, Paolo Serri, SystemC-based electronic system-level design space exploration environment for dedicated heterogeneous multi-processor systems, Microprocessors and Microsystems, Volume 72, 2020. [5] L. Pomante, G. Valente, V. Muttillo, D. Ciambrone. "HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems", In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS'2018), Budva, Montenegro, 2018.

ID	05
Title	Energy/Power-Aware System-Level Design Space Exploration for Heterogeneous Parallel Dedicated Systems
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	The work focuses on the extension of an ESL HW/SW Co-Design methodology in order to consider energy and power issues. In

	particular, the goal is to improve an existing DSE approach to suggest implementations that: - Satisfy both energy and timing requirements (or minimize energy consumption while satisfying timing requirements) - Satisfy both power and timing requirements (or minimize peak power dissipation while satisfying timing requirements) - Both of the previous ones
References	[1] L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC", IEEE Transactions on Computers, vol. 55, no. 5, May 2006. [2] L. Pomante, "System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems". IEEE International Conference on Application-specific Systems, Architectures and Processors, Santa Monica, Settembre 2011. [3] L. Pomante, P. Serri. "SystemC-based HW/SW Co-Design of Heterogeneous Multiprocessor Dedicated Systems". International Journal of Information Systems, Journal ISSN Online: 2356-5896, Vol. 1, July 2014. [4] Luigi Pomante, Vittoriano Muttillo, Marco Santic, Paolo Serri, SystemC-based electronic system-level design space exploration environment for dedicated heterogeneous multi-processor systems, Microprocessors and Microsystems, Volume 72, 2020. [5] L. Pomante, G. Valente, V. Muttillo, D. Ciambrone. "HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems", In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS'2018), Budva, Montenegro, 2018.

ID	06
Title	System-Level Design Space Exploration for Heterogeneous Parallel Dedicated Real-Time Systems
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	The work focuses on the extension of an ESL HW/SW Co-Design methodology in order to consider also real-time constraints. In particular, the goal is to improve an existing DSE approach to

	suggest implementations that are able to satisfy different kind of timing constraints: - Time to Completion - Time to Reaction - Extended Time to Reaction
References	[1] L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. "Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC", IEEE Transactions on Computers, vol. 55, no. 5, May 2006. [2] L. Pomante, "System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems". IEEE International Conference on Application-specific Systems, Architectures and Processors, Santa Monica, Settembre 2011. [3] L. Pomante, P. Serri. "SystemC-based HW/SW Co-Design of Heterogeneous Multiprocessor Dedicated Systems". International Journal of Information Systems, Journal ISSN Online: 2356-5896, Vol. 1, July 2014. [4] Luigi Pomante, Vittoriano Muttillo, Marco Santic, Paolo Serri, SystemC-based electronic system-level design space exploration environment for dedicated heterogeneous multi-processor systems, Microprocessors and Microsystems, Volume 72, 2020. [5] L. Pomante, G. Valente, V. Muttillo, D. Ciambrone. "HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems", In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS'2018), Budva, Montenegro, 2018. [6] V. Muttillo, G. Valente, D. Ciambrone, V. Stoico, and L. Pomante, "HEPSYCODE-RT: a Real-Time Extension for an ESL HW/SW Co-Design Methodology", Proceedings of the 10th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'18), ACM, New York, NY, USA, 2018, https://dl.acm.org/citation.cfm?id=3180670.

ID	07
Title	Quantum Genetic Algorithm for Design Space Exploration
Contacts	Vittoriano Muttillo (vittoriano.muttillo@univaq.it) Luigi Pomante (luigi.pomante@univaq.it)

Description	Genetic algorithms (GAs) are a class of evolutionary algorithms inspired by Darwinian natural selection. In the last decade, the possibility of emulating a quantum computer (a computer that uses quantum mechanical phenomena to perform data operations) has led to a new class of GAs known as 'Quantum Genetic Algorithms' (QGAs). The goals of the proposed work are the following ones: • to investigate the state of the art and available solutions for QGAs • to implement QGAs (partially or completely) • to extend the existing approaches for a GA used in a design space exploration within an electronic system-level HW/SW co-design flow • to perform experiments in simulation and/or on a real quantum processor (e.g., IBM Q)
References (Online)	https://github.com/ResearchCodesHub/QuantumGeneticAlgorithms https://www.punto-informatico.it/ibm-q-system-one-computer-quantistico/ https://qiskit.org/documentation/qc_intro.html
References	[1] Sofge, D.A. Prospective algorithms for quantum evolutionary computation. Proceedings of the Second Quantum Interaction Symposium (QI-2008), College Publications, Oxford, UK, 26-28 March, 2008. [2] Donald A. Sofge, Prospective Algorithms for Quantum Evolutionary Computation, Proceedings of the Second Quantum Interaction Symposium (QI-2008), College Publications, UK, 2008 [3] Laboudi, Zakaria & Chikhi, Salim. (2012). Comparison of Genetic Algorithm and Quantum Genetic Algorithm. International Arab Journal of Information Technology. 9. [4] Wu, Zheng-Guang, Wang, Huaixiao, Liu, Jianyong, Zhi, Jun, Fu, Chengqun, 2013, The Improvement of Quantum Genetic Algorithm and Its Application on Function Optimization, Mathematical Problems in Engineering, Hindawi Publishing Corporation [5] Lahoz-Beltra, Rafael. 2016. "Quantum Genetic Algorithms for Computer Scientists" Computers 5, no. 4: 24. [6] Giovanni Acampora, Autilia Vitiello, Implementing evolutionary optimization on actual quantum processors, Information Sciences, Volume 575, 2021, Pages 542-562

ID	08
Title	Parallel Genetic Algoritms and Parallel Evolutionary Algorithms for Design Space Exploration
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work focuses on DSE for heterogeneous embedded multiprocessor systems and attempts to introduce an improvement that reduces execution time using parallel programming languages (e.g., OpenMP) within the genetic algorithm or evolutionary approach. At the same time, we try to find better partitioning solutions and introduce the possibility to implement parallel genetic algorithms (e.g. distributed genetic algorithms on heterogeneous platforms). Specifically: - Introduction of parallel programming languages and approaches on CPU /GPU. - Exploit Parallel Genetic Algorithms (PGA) and Parallel Evolutionary Algorithms (PEA) on CPU /GPU. - Leverage reconfigurable and/or accelerated platforms for PGA/PEA (SoC such as Pynq boards, HLS tools, etc.)
References	[1] Vittoriano Muttillo, Paolo Giammatteo, Giuseppe Fiorilli, and Luigi Pomante. 2020. An OpenMP Parallel Genetic Algorithm for Design Space Exploration of Heterogeneous Multi-processor Embedded Systems. In Proceedings of the 11th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures / 9th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM'2020). Association for Computing Machinery, New York, NY, USA, Article 4, 1–6.

ID	09
Title	Multi-objective Optimization Metaheuristic Algorithms (MOMA) for Design Space Exploration
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work leads to the implementation of MOMA for DSE using metaheuristic or heuristic algorithms known in the literature. Specifically: - Analyze SOTA with respect to MOMA for DSE.

	- Select the solution to be implemented and integrate it into an existing DSE tool. - Analyze results and improve performance by means of specific metrics - Compare results with existing solutions
References	[1] Qi Liu, Xiaofeng Li, Haitao Liu, Zhaoxia Guo, Multi-objective metaheuristics for discrete optimization problems: A review of the state-of-the-art, Applied Soft Computing, Volume 93, 2020. [2] https://ewh.ieee.org/conf/wcci/2016/document/tutorials/cec1.pdf

ID	10
Title	Pareto Analysis and Optimization for Design Space Exploration
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work would use Pareto analysis and optimization metrics applied to DSE. Specifically: - Analysis of SOTA in conjunction with Pareto theory and analysis. - Implement/enhance/improve existing/new tools for Pareto analysis and optimization. - Improvement of the settings and steps of the metaheuristic approach of the DSE - Improve the performance of the tool with parallel languages (e.g. OpenMP) and architectures (e.g. CPUs, GPUs, FPGAs)
References	[1] Vittoriano Muttillo, Giuseppe Fiorilli, and Tania Di Mascio. 2019. Tuning DSE for Heterogeneous Multi-Processor Embedded Systems by means of a Self-Equalized Weighted Sum Method. In Proceedings of the 10th and 8th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM 2019). Association for Computing Machinery, New York, NY, USA, Article 1, 1–4. DOI:https://doi.org/10.1145/3310411.3310412 [2] https://ewh.ieee.org/conf/wcci/2016/document/tutorials/cec1.pdf

ID	11

Title	Machine learning for Multi-objective Optimization Problem (MOP) into a Design Space Exploration approach
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work leads to the solution of MOP for DSE using machine learning algorithms well known in the literature. Specifically: - Analyze SOTA with respect to ML for MOP. - Select a solution to be implemented and integrated into an existing DSE tool. - Analyze results and improve performance using specific metrics - Compare results with existing solutions
References	[1] Li, Kaiwen & Zhang, Tao & Wang, Rui. (2019). Deep Reinforcement Learning for Multi-objective Optimization. [2] R. G. Kim, J. R. Doppa and P. P. Pande, "Machine Learning for Design Space Exploration and Optimization of Manycore Systems," 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018, pp. 1-6, doi: 10.1145/3240765.3243483. [3] https://kaltura.stevens.edu/media/%22Design+Space+Exploration+with+Machine+Learning%22+with+Professor+Kishore+Pochiraju/1_86kwhwih/184962423

ID	12
Title	Design Space Exploration for Machine Learning techniques
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work leads to the introduction of DSE for machine learning techniques while improving performance and other NF constraints in the implementation of ML algorithms and approaches (e.g., regression trees, random forests, [deep] neural networks, etc.). Specifically: - Analyze SOTA in terms of DSE for ML. - Select a solution to implement and integrate with an existing DSE tool. - Analyze results and improve performance using specific metrics - Compare results with existing solutions

References	[1] A. Colucci et al., "A Fast Design Space Exploration Framework for the Deep Learning Accelerators: Work-in-Progress," 2020 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2020, pp. 34-36, doi: 10.1109/CODESISSS51650.2020.9244038. [2] https://scholarworks.iupui.edu/bitstream/handle/1805/24768/FINAL%20Prasham_Shah_Thesis%20.pdf?sequence=1&isAllowed=y

ID	13
Title	High-Level Synthesis error estimation and correction using AI/ML algorithms
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work has led to reducing the errors associated with HLS tools and RTL simulations using machine learning (i.e., based on data results): Specifically: - Analyze SOTA in terms of HLS tool and RTL simulation errors. - Select solution to be implemented and integrate with existing data extraction tool. - Analyze results and improve performance using specific machine learning techniques - Compare the results with existing solutions
References	[1] S. Dai, Y. Zhou, H. Zhang, E. Ustun, E. F. Y. Young and Z. Zhang, "Fast and Accurate Estimation of Quality of Results in High-Level Synthesis with Machine Learning," 2018 IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2018, pp. 129-132.

ID	14
Title	HW/SW Performance Estimation using AI/ML algorithms
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	In the initial design phases of an embedded system, it is essential to assist designers with metrics obtained through preliminary analysis. It is even more important to know which initial parameters of the

	embedded system (HW or SW) influence these metrics. The main feature of an embedded system that developers usually need to measure is the execution time of the embedded SW (i.e., functions), which is used to describe the final system performance (i.e., the timing performance metric). Evaluating such a metric is often a critical task, relying on several different techniques at different levels of abstraction. Other important metrics relate to power/energy consumption, area occupationt (HW and/or SW), manufacturing and/or NRE costs, etc. Moreover, in the era of Big Data, the use of machine learning methods can be a good alternative to the classical methods used to evaluate or estimate system performance metrics. In such a context, this work aims to: - Analyze SOTA in terms of system performance prediction. - Extend a framework based on the use of machine learning methods to compute system performance metrics and predictions. - Analyze the results and improve performance using specific machine learning techniques. - Compare the results with existing solutions in terms of simulation accuracy and execution time.
References	[1] Vittoriano Muttillo, Paolo Giammatteo, and Vincenzo Stoico. 2021. Statement-Level Timing Estimation for Embedded System Design Using Machine Learning Techniques. In Proceedings of the ACM/SPEC International Conference on Performance Engineering (ICPE '21). Association for Computing Machinery, New York, NY, USA, 257–264.

ID	15
Title	Model-Driven Engineering and DevOps practices for HW/SW Co-Design
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it) Vincenzo Stoico (vincenzo.stoico@graduate.univaq.it)
Description	This work is closely related to an ongoing European project called AIDOaRt (https://www.aidoart.eu/). The objectives relate to SOTA analysis, MDE and DevOps practices applied to HW /SW co-design, and industrial and/or academic applications in the context of European project use cases.
References	[1] R. Eramo et al., "AIDOaRt: AI-augmented Automation for DevOps, a Model-based Framework for Continuous Development in

	Cyber-Physical Systems," 2021 24th Euromicro Conference on Digital System Design (DSD), 2021, pp. 303-310.

ID	16
Title	Model-Driven HW/SW Co-Design methodology and EDA tool for code generation and traceability
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it) Vincenzo Stoico (vincenzo.stoico@graduate.univaq.it)
Description	This work aims to extend/refine/improve an existing MDE framework for code generation and traceability in the context of system-level automation approaches to electronic design.
References	[1] D. Di Pompeo, E. Incerto, V. Muttillo, L. Pomante, G. Valente. 2017. An Efficient Performance-Driven Approach for HW/SW Co-Design. In Proceedings of the 8th ACM/SPEC on International Conference on Performance Engineering (ICPE '17). Association for Computing Machinery, New York, NY, USA, 323–326.

ID	17
Title	Electronic System Level HW/SW Co-Simulation
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Vittoriano Muttillo (vittoriano.muttillo@univaq.it)
Description	This work aims to extend/refine/improve an existing SystemC-based simulator (HEPSIM) by focusing on one or more of the following features: - Introduction of arbiters for physical links - Improved concurrency analysis - Comparison with TLM and other tools (e.g., Intel Co-Fluent) - Use cases refinement/development - Multi-MOC simulation - Multi-core extension - Re-engineering (e.g., channel inheritance) - Extensions to support DSE at run-time
References	[1] L. Pomante, P. Serri. “SystemC-based HW/SW Co-Design of Heterogeneous Multiprocessor Dedicated Systems”. International Journal of Information Systems, Journal ISSN Online: 2356-5896, Vol. 1, July 2014. [2] Luigi Pomante, Vittoriano Muttillo, Marco Santic, Paolo Serri, SystemC-based electronic system-level design space exploration

	environment for dedicated heterogeneous multi-processor systems, Microprocessors and Microsystems, Volume 72, 2020. [3] L. Pomante, G. Valente, V. Muttillo, D. Ciambrone. “HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded Systems”, In 6th EUROMICRO/IEEE Workshop on Embedded and Cyber-Physical Systems (ECYPS’2018), Budva, Montenegro, 2018.