

<b>Title</b>	Run-time monitoring of software execution of Zynq Ultrascale+
<b>Contacts</b>	Giacomo Valente ( <a href="mailto:giacomo.valente@univaq.it">giacomo.valente@univaq.it</a> )
<b>Description</b>	The work aims at developing software routines able to monitor the execution of software on a heterogeneous platform widely used in aerospace (Zynq Ultrascale +). The monitoring systems are already built inside the hardware platform, and will be opportunely controlled by the developed software routines.

<b>Title</b>	SoC for spatial audio
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<b>Description</b>	The work focuses on the analysis of binaural rendering solutions for implementation on a system-on-chip platform <ul style="list-style-type: none"> <li>- to study available solutions for binaural rendering</li> <li>- to implement (partially or completely) the experiment in reference [1]</li> <li>- to extend the previous experimentation to other rendering solutions</li> </ul>
<b>References</b>	[1] Fohl, Wolfgang & Reichardt, Jürgen & Kuhr, Jan & Hamburg, Haw. (2010). A System-On-Chip Platform for HRTF-Based Realtime Spatial Audio Rendering.

<b>Title</b>	MONICA tool: Design and Development of an "on-the-job" Technology-Enhanced Learning tool dedicated to Cyber-Physical System Designers.
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<b>Description</b>	The work aims at designing and implementing an "on-the-job" Technology-Enhanced Learning tool able to meet the needs of Cyber-Physical system designers called MONICA tool. This tool aims to support these people in designing complex Cyber-Physical Systems while promoting the continuous learning of practical knowledge and skills. The final product will be a Web Integrated Development Environment-based Application whose design stage will encompass several different aspects, including user interface design (UI) and usability (UX), using the User-Centered Design approach.

<b>Title</b>	DRAM memory stress test under Dynamic Partial Reconfiguration process on Zynq Ultrascale+
<b>Contacts</b>	Giacomo Valente ( <a href="mailto:giacomo.valente@univaq.it">giacomo.valente@univaq.it</a> )
<b>Description</b>	The work aims at developing a system with four hardware memory stress modules and one accelerator implemented at run-time through the Dynamic Partial Reconfiguration process. The system serves to characterize the impact in terms of latency on the DPR process.

<b>Title</b>	Building ROS (Robot Operating System) compliant actor on FPGA
<b>Contacts</b>	Giacomo Valente ( <a href="mailto:giacomo.valente@univaq.it">giacomo.valente@univaq.it</a> )
<b>Description</b>	The work aims at developing a ROS compliant actor on FPGA, constituting the foundation of controlling modern robots. The work will be performed following the tutorial reported at the link: <a href="https://github.com/Lien182/ReconROS">https://github.com/Lien182/ReconROS</a>

<b>Title</b>	Runtime shaping of software performance through quality of service knobs
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<b>Description</b>	The work aims at developing software routines able to shape, at run-time, the performance of some applications under execution on a general purpose processors (GPPs). The GPP involved is from aerospace applications and it provides some internal knobs to control the processor components and slowdown application execution. The work will be performed following the tutorial reported at the link: <a href="https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/688128001/Traffic+Shaping+of+HP+Ports+on+Zynq+UltraScale">https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/688128001/Traffic+Shaping+of+HP+Ports+on+Zynq+UltraScale</a>