Advanced (e.g., high-performance, reconfigurable, multi-processors, heterogeneous, real-time, monitored) embedded platforms

C/C++ and/or VHDL-based FPGA environments for the development/exploitation of advanced embedded applications.

Title	Run-time monitoring of software execution of Zynq Ultrascale+ ONLY FOR MASTER THESIS
Contacts	Giacomo Valente (giacomo.valente@univaq.it)
Description	The work aims at developing software routines able to monitor the execution of software on a heterogenoeus platform widely used in aerospace (Zynq Ultrascale +). The monitoring systems are already built inside the hardware platform, and will be opportunely controlled by the developed software routines.

Title	SoC for spatial audio
Contacts	Luigi Pomante (luigi.pomante@univaq.it) Claudia Rinaldi (claudia.rinaldi@univaq.it)
Description	The work focuses on the analysis of binaural rendering solutions for implementation on a system-on-chip platform - to study available solutions for binaural rendering - to implement (partially or completely) the experiment in reference [1] - to extend the previous experimentation to other rendering solutions
References	[1] Fohl, Wolfgang & Reichardt, Jürgen & Kuhr, Jan & Hamburg, Haw. (2010). A System-On-Chip Platform for HRTF-Based Realtime Spatial Audio Rendering.

Title	MONICA tool: Design and Development of an “on-the-job” Technology-Enhanced Learning tool dedicated to Cyber-Physical System Designers.
Contacts	**Thesis Supervisor: Tania Di Mascio (tania.dimascio@univaq.it)** Giacomo Valente (giacomo.valente@univaq.it) Federica Caruso (federica.caruso1@graduate.univaq.it
Description	The work aims at designing and implementing an "on-the-job" Technology-Enhanced Learning tool able to meet the needs of Cyber-Physical system designers called MONICA tool. This tool aims to support these people in designing complex Cyber-

	Physical Systems while promoting the continuous learning of practical knowledge and skills. The final product will be a Web Integrated Development Environment-based Application whose design stage will encompass several different aspects, including user interface design (UI) and usability (UX), using the User-Centered Design approach.

Title	DRAM memory stress test under Dynamic Partial Reconfiguration process on Zynq Ultrascale+ ONLY FOR MASTER THESIS
Contacts	Giacomo Valente (giacomo.valente@univaq.it)
Description	The work aims at developing a system with four hardware memory stress modules and one accelerator implemented at run-time through the Dynamic Partial Reconfiguration process. The system serves to characterize the impact in terms of latency on the DPR process.

Title	Building ROS (Robot Operating System) compliant actor on FPGA
Contacts	Giacomo Valente (giacomo.valente@univaq.it)
Description	The work aims at developing a ROS compliant actor on FPGA, constituting the foundation of controlling modern robots. The work will be performed following the tutorial reported at the link: https://github.com/Lien182/ReconROS

Title	Runtime shaping of software performance through quality of service knobs
Contacts	Giacomo Valente (giacomo.valente@univaq.it)
Description	The work aims at developing software routines able to shape, at run-time, the performance of some applications under execution on a general purpose processors (GPPs). The GPP involved is from aerospace applications and it provides some internal knobs to control the processor components and slowdown application execution. The work will be performed following the tutorial reported at the link: https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/688128001/Traffic+Shaping+of+HP+Ports+on+Zynq+UltraScale

Title	Advanced development and verification of a pacemaker
Contacts	Luigi Pomante (luigi.pomante@univaq.it)

Description	The work aims at improving the implementation and the verification of a pacemaker (i.e., one of the most famous cyber-physical systems). In particular, projects related to this work will focus on one or more of the following activities: porting of the current implementation from ATMEGA328P (Arduino-based) to soft-cores on FPGA (e.g., Microblaze) or to SoC (e.g., ARM-based ZYNQ); integration of a heart model in the loop for advanced verification; integration of a HW monitoring system for run-time verification; comparison of the performances of different implementations (i.e., hand-made vs automatically suggested by an HW/SW co-design flow).

Title	Dynamic partial reconfiguration flow on Zynq Ultrascale+ ONLY FOR MASTER THESIS
Contacts	Giacomo Valente (giacomo.valente@univaq.it)
Description	The work aims at implementing two different accelerators on FPGA and to switch them at runtime using the Dynamic Function Exchange feature of FPGAs (https://www.xilinx.com/products/design-tools/vivado/high-level-design.html#dfx)