JOINTER

JOining flexIble moNitors wiTh hEterogeneous architectuRes

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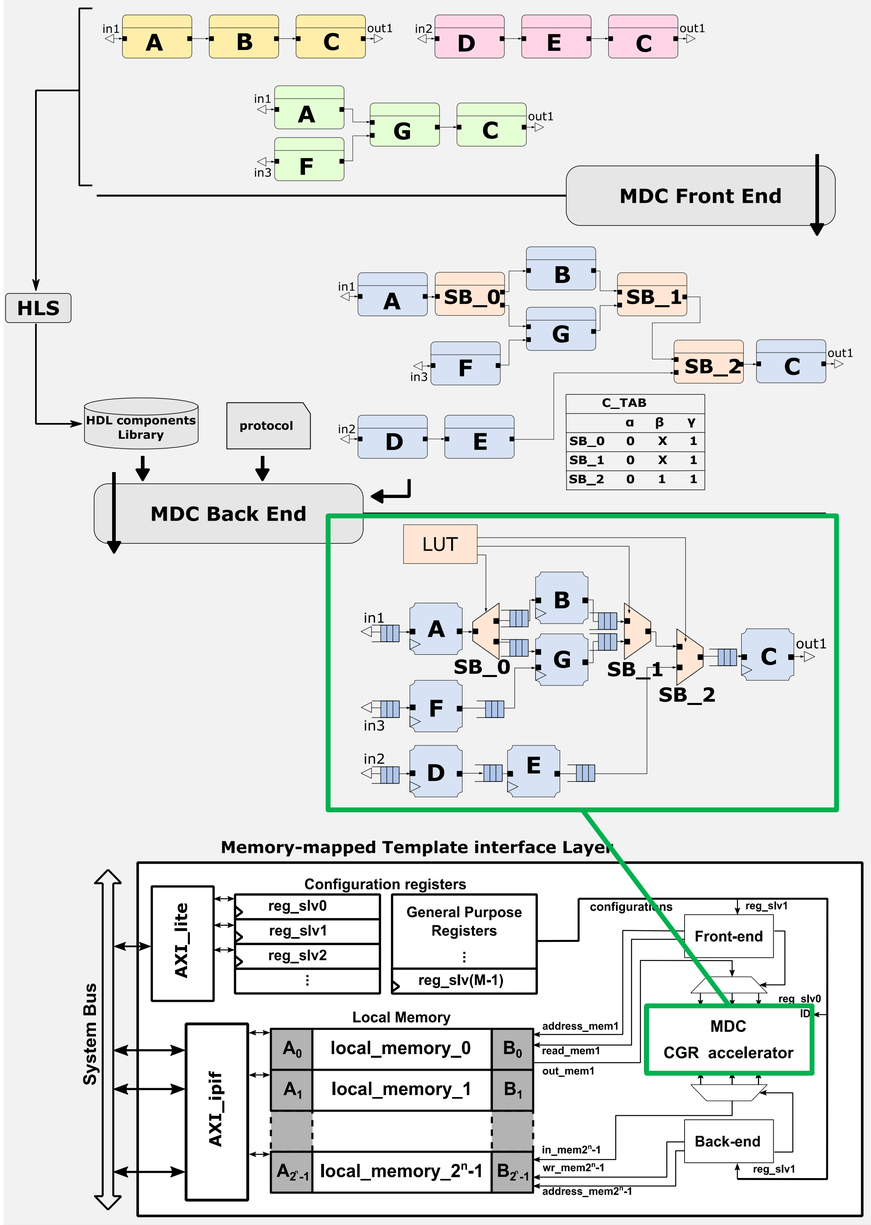
Motivation: taming the runtime observation of heterogeneous systems

As embedded systems grow more complex and shift toward heterogeneous architectures, understanding workload performance characteristics becomes increasingly difficult. In this regard, run-time monitoring systems can support on obtaining the desired visibility to characterize a system. This demo presents a framework that allows to develop complex heterogeneous architectures composed of programmable processors and dedicated accelerators on FPGA, together with customizable monitoring systems, keeping under control the introduced overhead.

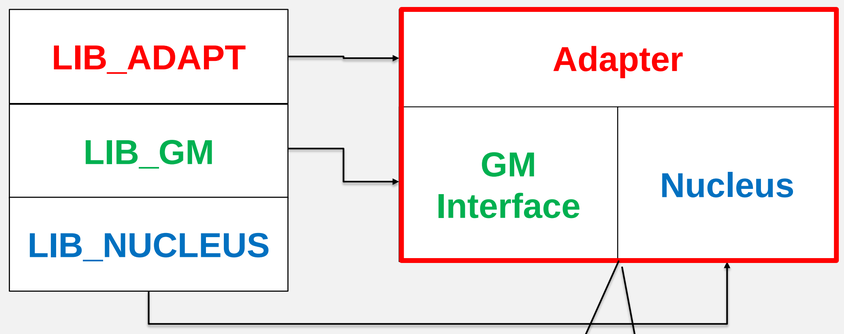
Jointer Foundations: accelerators and monitoring systems

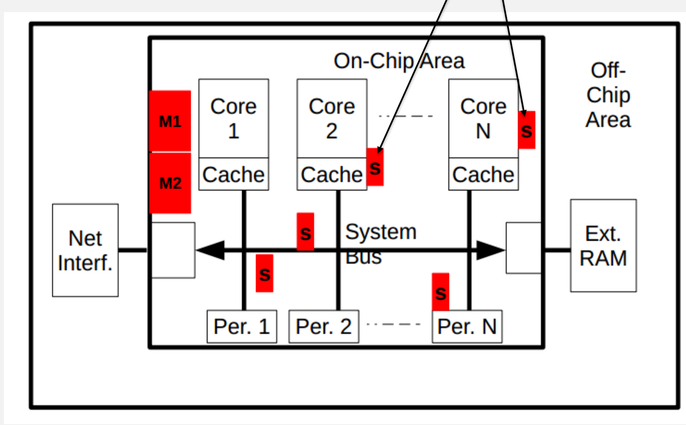


The **Multi-Dataflow Composer [1]** (**MDC**) tool automates the development of **Coarse-Grain Virtual Reconfigurable Circuits** (CG-VRCs) by taking as input a set of dataflow networks and merging them to generate Xilinx compliant accelerators.

https://github.com/mdc-suite/mdc

The **A**dapt**I**ve **P**otential **H**ardware profiling **S**ystem **[2]** (**AIPHS**) is a library of elements to **compose hardware monitoring systems** for reconfigurable architectures, in order to support on the characterization of platforms from the point of view of different metrics. It brings **flexibility** and **reusability** in the usage of hardware monitoring systems.



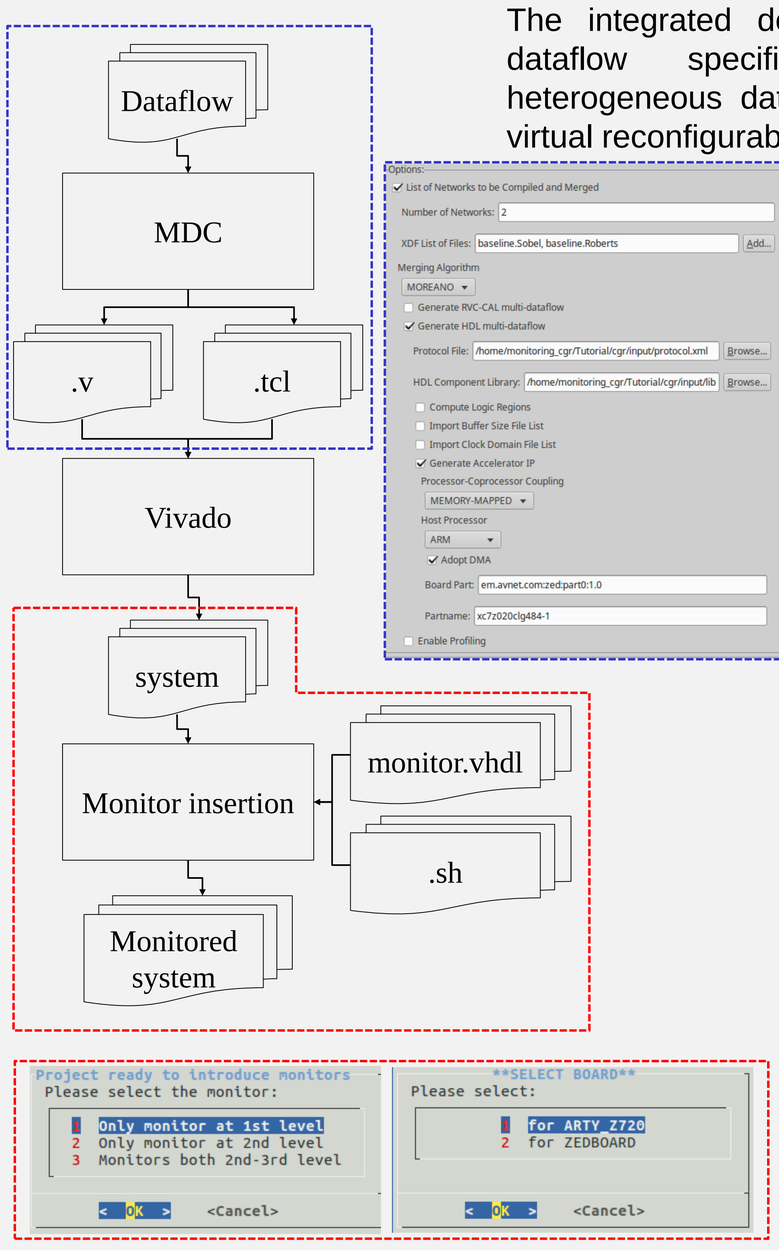


- **Adapter** is the part to be changed to monitor different interconnections
- **Nucleus** is the part that contains the logic to measure metrics
- **GM Interface** is the part that initializes and sends data to a central information collector

[1] F. Palumbo et al. 2017. Power-Awarness in Coarse-Grained Reconfigurable Multi-Functional Architectures: a Dataflow Based Strategy. Journal of Signal Processing Systems 87, 1 (01 Apr 2017), 81–106. doi:10.1007/s11265-016-1106-9

[2] G. Valente et al., "A flexible profiling sub-system for reconfigurable logic architectures", in Proceedings of PDP 2016 (in press), February 2016.

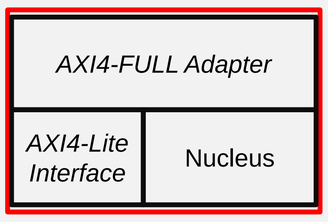
Jointer Framework: easy and flexible monitoring heterogeneous systems



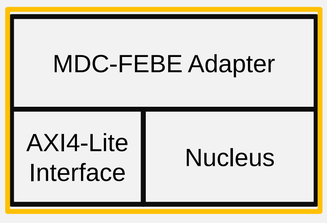
The integrated design flow, starting from dataflow specifications generates a heterogeneous dataflow based coarse-grain virtual reconfigurable system.

In this heterogeneous system the monitors are inserted at different levels in a composable way.

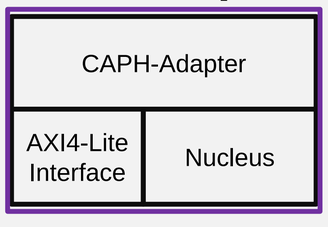
Monitor Level 1 - Bus Level



Monitor Level 2 - Interface Level



Monitor Level 3 - Data-path Level



This composable monitoring approach, here demonstrated in a dataflow context, is generic and valid for every kind of heterogeneous processor-coprocessor system.

The 1st level monitor is able to count the number of writing and reading transactions happening on AXI4-FULL bus, that are within a predefined range.

The 2nd level monitor is able to measure the latency of the acceleration, enforcing the monitoring action to characterize the performance of the acceleration.

The 3rd level monitor is able to runtime verify the happening of certain events, enforcing the monitoring action to verity the correctness of the execution.

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