HEPSYCODE-MC

Electronic System-Level Methodology for HW/SW Co-Design of Mixed-Criticality Embedded Systems

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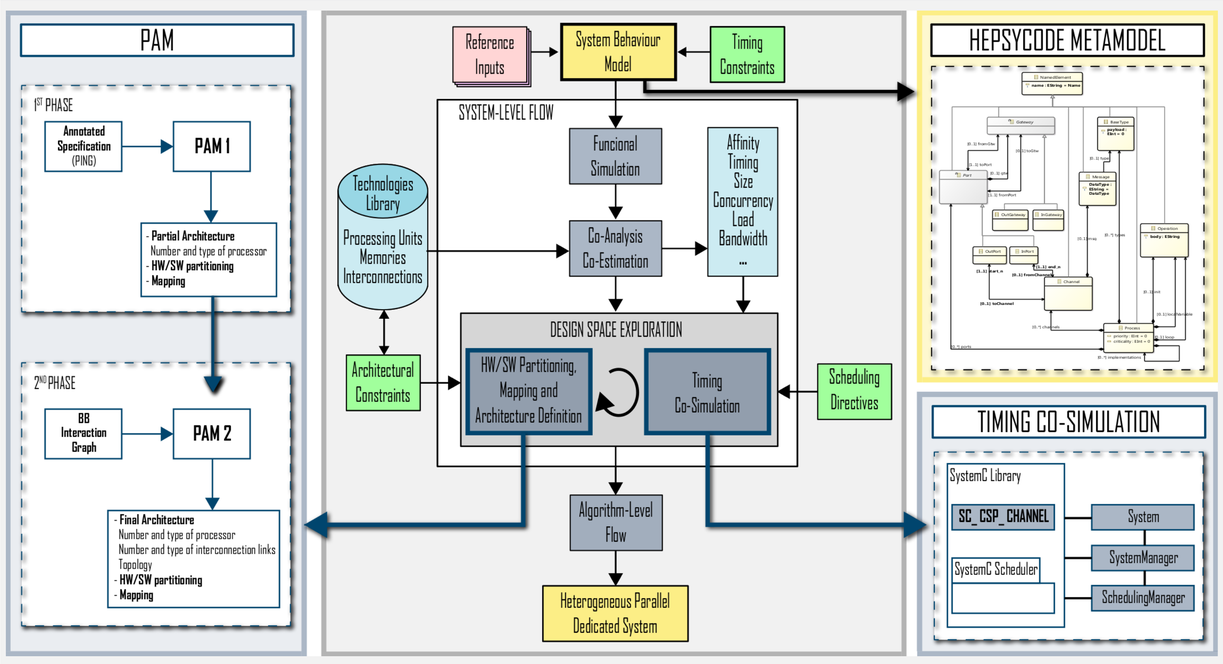
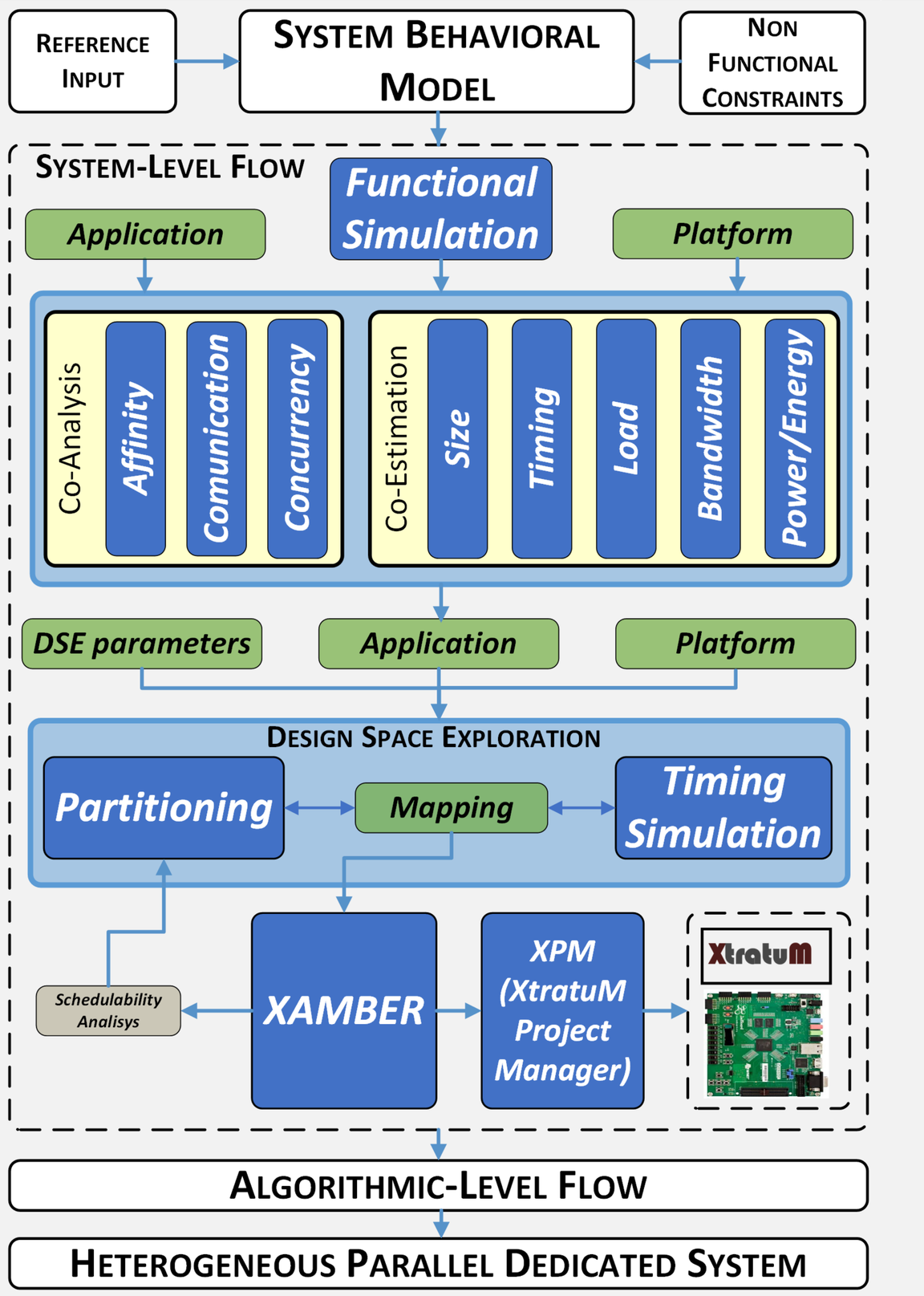
Introduction

- The early embedded system design activities deal with the modeling of **F/NF requirements** and their its validation before the final implementation. Designers use system-level models to identify the more adequate HW/SW resources allocation by simulating system behavior. Dedicated SW tools become mandatory to support designers to reduce costs and overall complexity of systems development.
- This work is focused on "**Model-Based ESL HW/SW Co-design**" and on the development of a framework for modeling, analysis and validation of **Mixed-Criticality Embedded Systems**. It is based on mixed-criticality requirements analysis, and related estimations and simulations, defined in the context of several European research projects.
- In this work it is proposed an **Electronic System-Level HW/SW Co-Design methodology**, and related tools, to design "**Heterogeneous Parallel Embedded Systems**" (e.g. multi-core systems, multi-processor systems, network-on-chip) for **Mixed-Criticality applications**.
- Starting from the **System Behavior Specification**, **Timing** and **Mixed-Criticality constraints**, the proposed approach aims to suggest the *HW/SW partitioning, the architecture and the mapping* of the partitioned entities onto the HW components, by means of a **Design Space Exploration** step able to consider also Hypervisor-based SW Partitions. The main idea is to drive the DSE to satisfy performance requirements while avoiding to have processes with different criticality levels allocated on the same (shared) partition/processor/core.

HEPSYCODE HW/SW Co-Design Flow

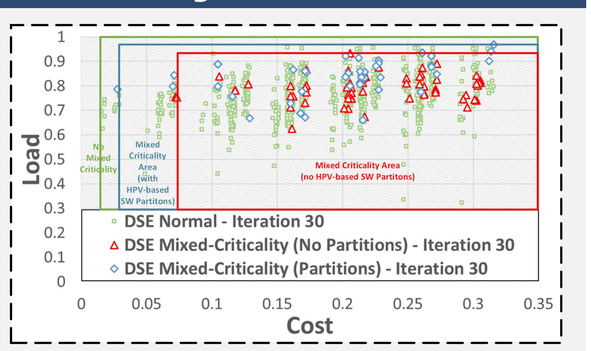


HEPSYCODE Framework

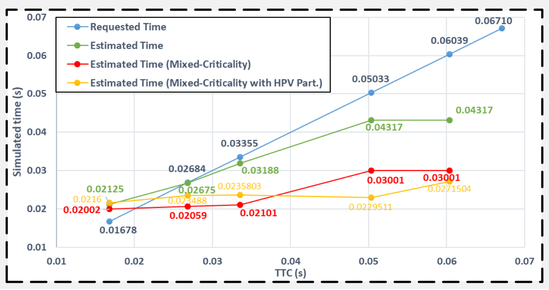


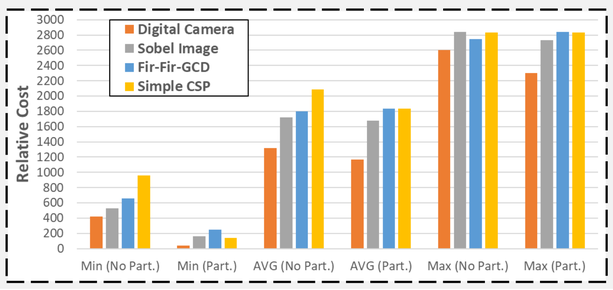
HEPSYCODE Analysis

Iteration	Cost	Load	Architecture bb_1	bb_2	bb_3 (1)	bb_3 (2)	bb_4	bb_5	PAM1 Execution Time
0	0.072	0.7614	1	2	1	2	1	0	0.0015 s
1	0.072	0.7578	1	2	1	2	1	0	0.0022 s
2	0.010	0.6951	2	2	0	1	1	0	0.0035 s
6	0.010	0.6951	2	2	0	1	2	0	0.0035 s
10	0.072	0.6573	1	2	1	1	1	0	0.0083 s
15	0.095	0.5899	2	2	0	0	2	0	0.0131 s
22	0.050	0.5740	1	2	0	0	1	0	0.0295 s
25	0.159	0.4486	1	1	2	0	0	1	0.0556 s
32	0.027	0.5562	1	2	1	3	0	0	0.2064 s
34	0.115	0.4598	2	1	0	4	0	1	0.2698 s
40	0.058	0.4559	1	1	4	0	1	0	0.6618 s
44	0.058	0.4559	1	1	4	0	1	0	1.2248 s
60	0.068	0.3198	0	1	1	4	0	0	11.959 s
100	0.068	0.3198	0	1	1	4	0	0	35.443 s



Solution	ω_{Cost}	$\omega_{Affinity}$	ω_{Load}	$\omega_{Parallelism}$	TTC	Architecture bb_1	bb_2	bb_3 (1)	bb_3 (2)	bb_4	bb_5	HEPSIM Simulated Time	Cost	Hyperplan laps
1	0.25	0.25	0.25	0.25	$0.9 \times T_{REF}$	1	2	0	2	1	0	0.0271504 s	560	26
2	0.25	0.25	0.25	0.25	$0.75 \times T_{REF}$	1	2	2	0	0	0	0.0229511 s	160	22
3	0.25	0.25	0.25	0.25	$0.5 \times T_{REF}$	2	2	1	1	0	0	0.0235803 s	260	-
4	0.25	0.25	0.25	0.25	$0.4 \times T_{REF}$	1	1	2	0	0	0	0.023488 s	140	42
5	0.25	0.25	0.25	0.25	$0.25 \times T_{REF}$	2	2	2	0	1	0	0.0216 s	560	93





Conclusion and Future Work

This work has presented an ESL HW/SW Co-Design approach able to take into account mixed-criticality constraints. The presented methodology, design flow and framework are able to drive the designer from the input specification to the final implementation solution. The Framework allows to (semi)-automatically generate solutions that are easily integrable with other tools that assist the user to finalize the configuration of partitioned systems, like **Xamber**, that generates the configuration file needed by a hypervisor to execute the system (i.e. **Xtratum** Hypervisor Software technology).

FUTURE WORK: (1) to integrate other external tools to enhance HEPSYCODE functionality, (2) to improve hierarchical scheduling implementation considering more detailed hypervisor issues, (3) to exploit parallel programming techniques for parallel evolutionary approach.

Acknowledgements

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