ELS HW/SW Co-Design Methodology for Mixed-Criticality and Real-Time Embedded Systems

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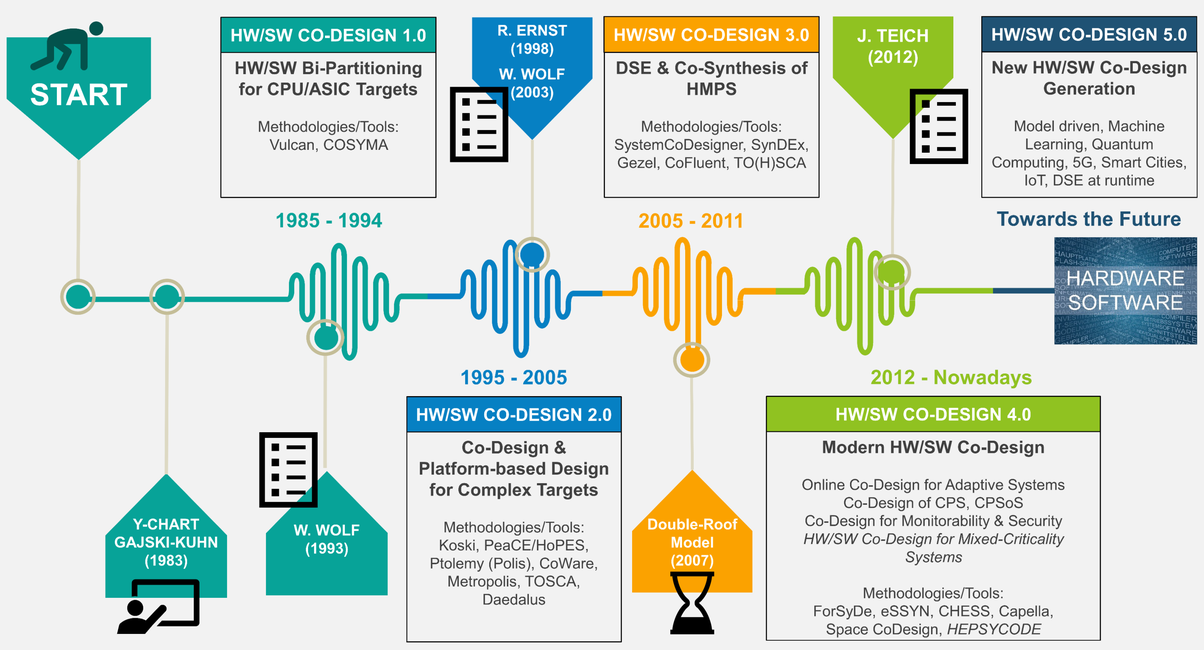
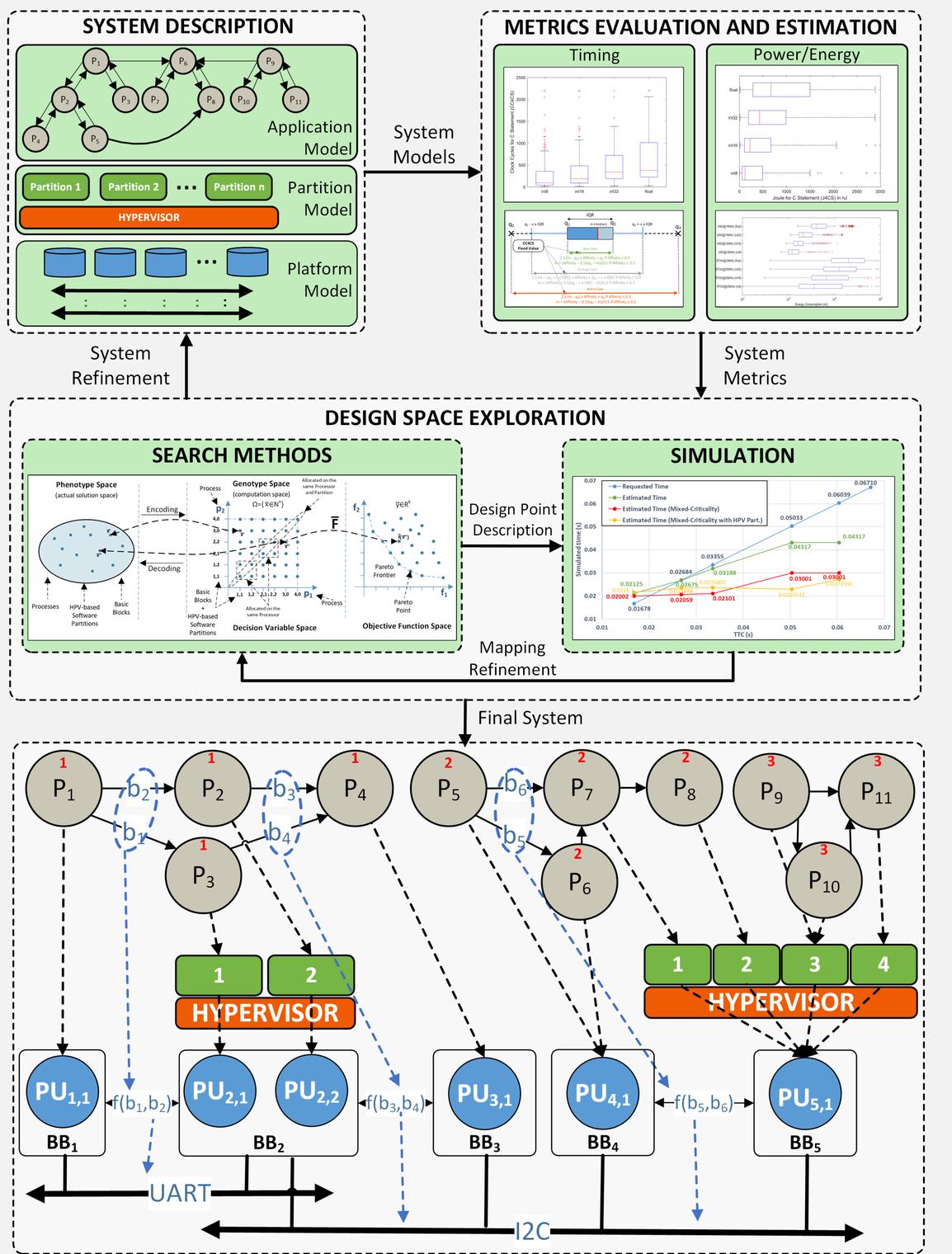
Ph.D. Work Goals

- Analysis of **mixed-criticality** embedded systems with focus on HW/SW technologies, architectures and components allowing the correct execution of mixed-criticality applications by means of spatial and/or temporal isolation techniques;
- Definition of an **ESL HW/SW Co-Design Methodology** based on models at different levels of abstraction (abstract formal model, concrete behavioral/functional models, Electronic System-Level specification);
- Development of an **ESL HW/SW Co-Design Framework** to automatize design activities while trying to optimize different conflicting metrics;
- Injection of **Real-time** and **Mixed-Criticality constraints** into the methodology, considering also **hypervisor** technologies;
- Improvement of **SystemC timing simulator** to check F/NF requirements, considering also **hypervisor** technologies by means of a **hierarchical scheduling** approach;
- **Validation** and **verification** of the methodologies considering representative use cases and integration of **external tool** for extra functionalities (e.g., schedulability analysis, HW/SW synthesis, hypervisor configuration and code generation etc.);

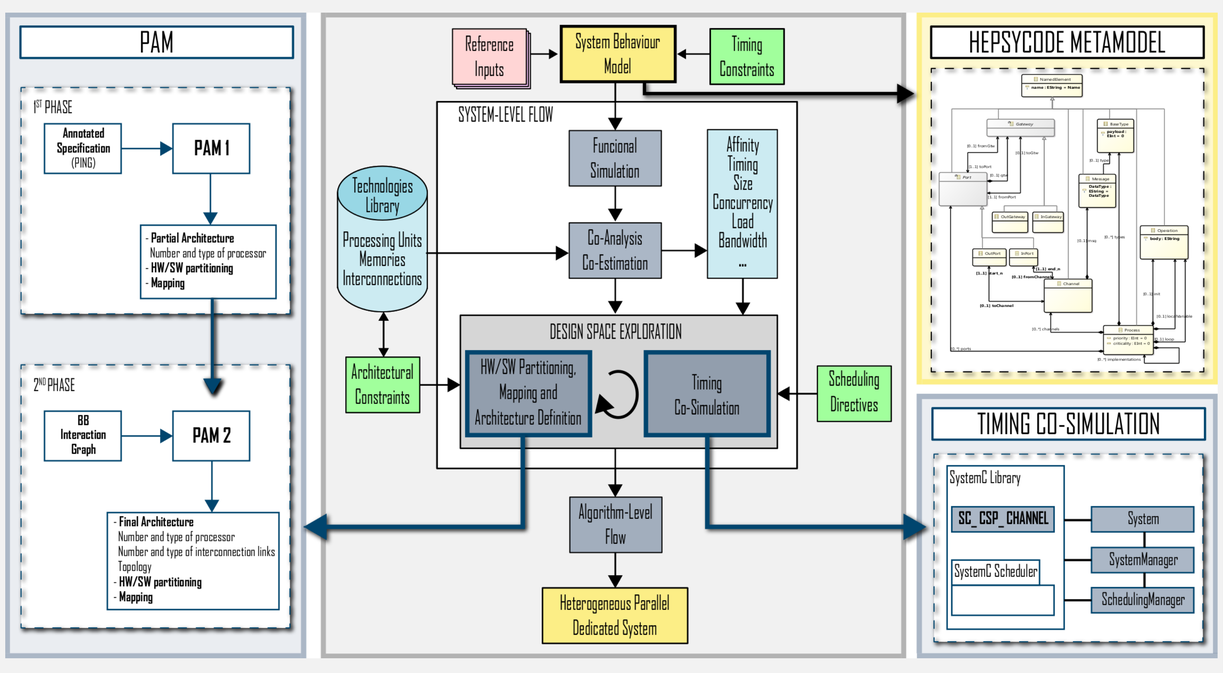
HW/SW Co-Design Timeline



HEPSYCODE Methodology



HEPSYCODE HW/SW Co-Design Flow



Conclusion and Future Work

This Ph.D. work has presented an ESL HW/SW Co-Design approach able to take into account mixed-criticality and real-time constraints. The presented methodology, design flow and framework are able to drive designers from the input specification to the final implementation solution, while exploiting several ESL design space exploration and analysis tools.

FUTURE WORK: (1) to integrate other external tools to enhance HEPSYCODE functionality, (2) to improve hierarchical scheduling implementation considering more detailed hypervisor issues, (3) to exploit parallel programming techniques for parallel evolutionary approach.

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[6]Hepsycode: HW/SW CO-DEsign of HEterogeneous Parallel dedicated SYstems, www.hepsycode.com

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