Criticality-aware Design Space Exploration for Mixed-Criticality Embedded Systems

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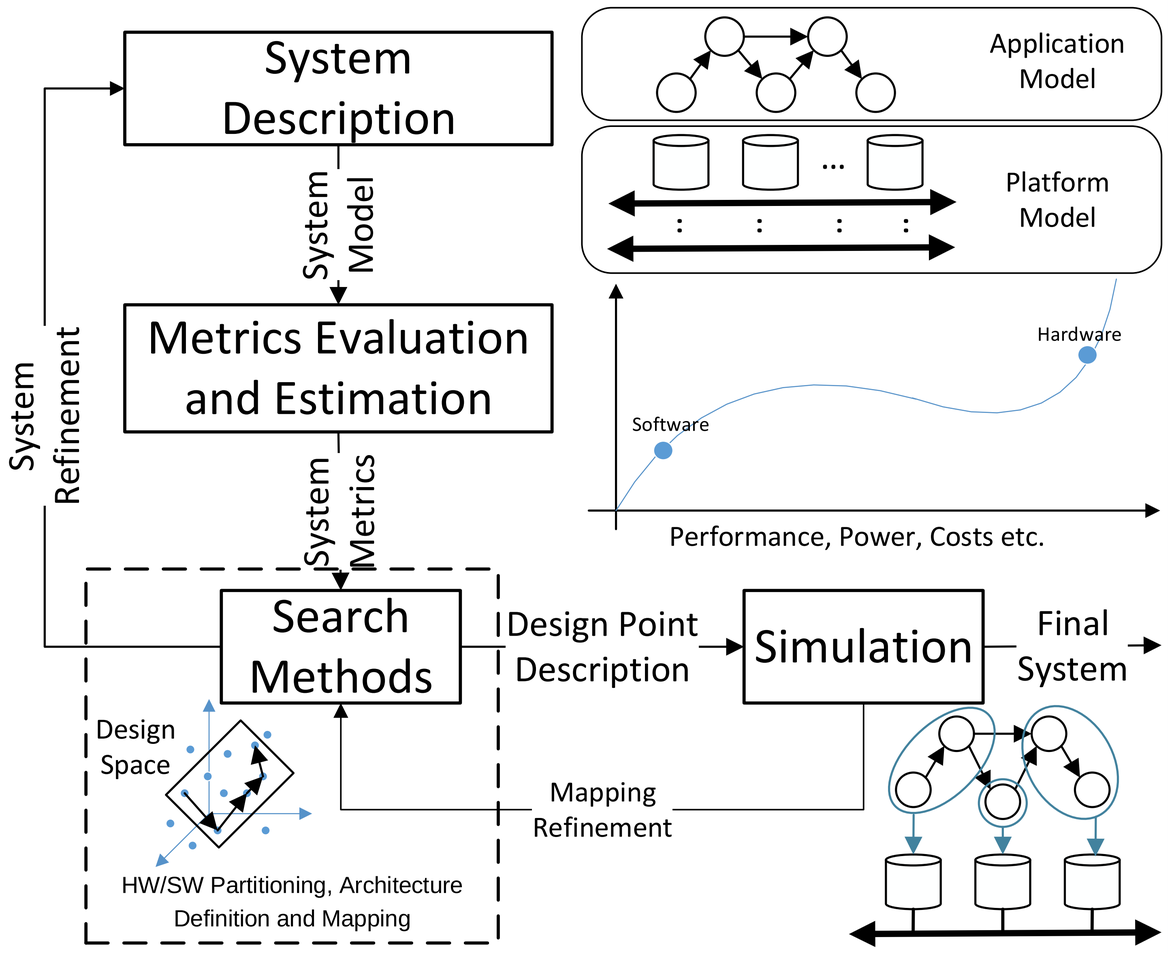
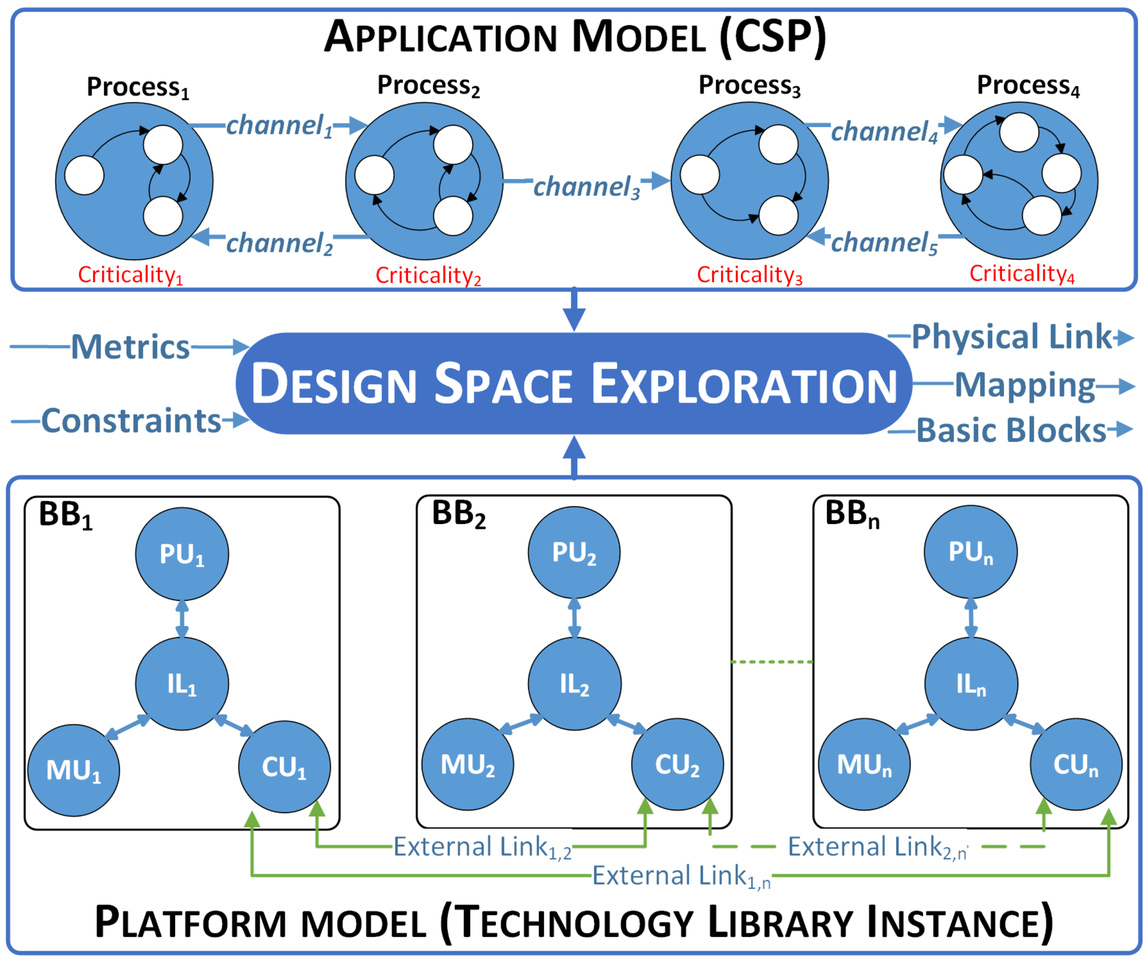
Introduction

- The early embedded system design activities are to model F/NF requirements and to validate them before final implementation. Designers use system-level models to identify best HW/SW resources allocation by simulating system behavior. Proper SW tools are fundamental to support designers to reduce costs and overall complexity of systems development.
- In such a context, this work is focused on the development of a framework for modeling, analysis and validation of mixed-criticality systems, through the use of software tools for "*Model-Based ESL HW/SW Co-design*" [1][2], refined to use estimates, metrics and simulations that consider mixed-criticality requirements, defined in the context of several European project [3].
- An Electronic System-Level HW/SW Co-Design methodology, and related tools, to design "*Heterogeneous Parallel Embedded Systems*" (e.g. multi-core systems, multi-processor systems, network-on-chip) for Mixed-Criticality applications has been proposed.
- Starting (at least) from the System Behavior Specification, Timing and Mixed-Criticality constraints, the proposed approach aims to suggest the HW/SW partitioning, the architecture and the mapping of the partitioned entities onto the HW components by means of the Design Space Exploration step (i.e. HW/SW partitioning, architecture definition and mapping)
- The main idea is to drive the DSE to avoid having processes with different criticality levels allocated on the same (shared) processor/core

HW/SW Co-Design Framework



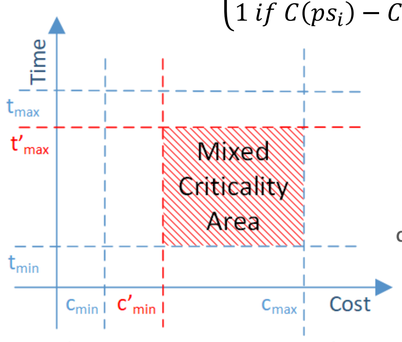
DSE Approach



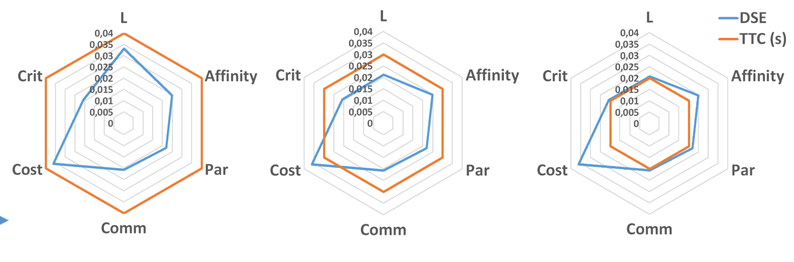
Mixed-Criticality Constraints

- DSE for mixed-criticality parallel embedded platforms:
  - A. Initialization step
    1. Reduce the starting random population deleting unfeasible individuals
    2. Create a starting constrained random population with only feasible individuals
  - B. Crossover and Mutation steps
    1. Avoid the generation of unfeasible individuals while generating only valid solutions, otherwise no result will be released
    2. Avoid the generation of unfeasible individuals while trying to generate a minimum (or maximum) amount of feasible individual
    3. Exploit the *Criticality Index:*

$$X_{CRIT} = \begin{cases} 0 \; if \; C(ps_i) - C(ps_j) = 0 \wedge ps_i \in pu_x \wedge ps_j \in pu_y \wedge pu_x = pu_y \\ 1 \; if \; C(ps_i) - C(ps_j) > 0 \wedge ps_i \in pu_x \wedge ps_j \in pu_y \wedge pu_x = pu_y \\ 1 \; if \; C(ps_i) - C(ps_j) = 0 \wedge ps_i \in pu_x \wedge ps_j \in pu_y \wedge pu_x \neq pu_y \end{cases}$$



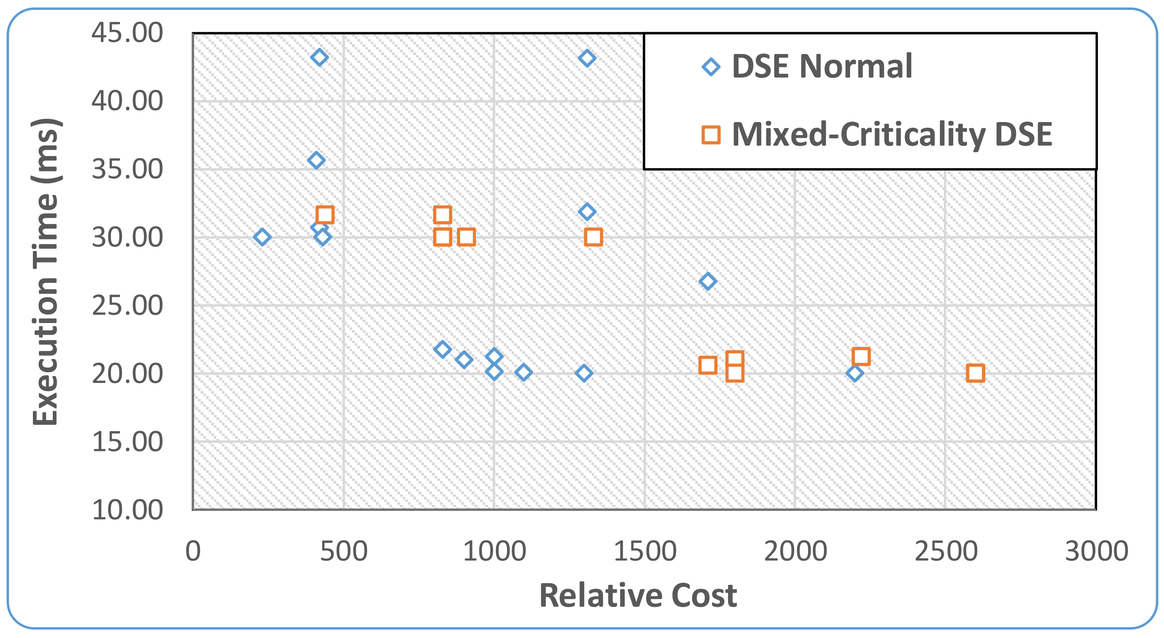
Design Space Representation with MC Requirements



Simulated Time with respect to different weights: the only metrics that badly drives the DSE with respect to timing performance is the *Cost Index* metrics

Preliminary Results

- Figure below shows a subset of solutions suggested by the DSE while considering a reference application and different weights and timing requirements, with and without MC constraints.
- Pareto set with no MC constraints (blue rhombuses more to the left) have solutions with a lower cost with respect to the one with MC constraints (orange squares).



Conclusion and Future Work

- This work has proposed a criticality-driven design space exploration for mixed-criticality heterogeneous parallel embedded systems.
- By introducing the *Criticality Index* into an evolutionary algorithm, the DSE suggests solutions that fulfill input constraints avoiding allocating applications with different levels of criticality on the same shared resource.
- Future works involve the introduction into the DSE also the concept of SW partitions in order to allow modeling Hypervisors technologies [4].
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Hepsycode
www.hepsycode.com

Reference

[1] L. Pomante, "HW/SW co-design of dedicated heterogeneous parallel systems: an extended design space exploration approach," Computers & Digital Techniques, IET, vol.7, no.6, pp.246,254, 2013
[2] L. Pomante, C. Bolchini, F. Salice, D. Sciuto. "Reliability Properties Assessment at System Level: a Co-Design Framework", Journal of Electronic Testing - Theory and Application (JETTA), Kluwer Academic Publishers, The Netherlands, Vol. 18, no. 3, p. 351-356, 2002.
[3] L. Pomante, V. Muttillo, G. Valente, F. Federici, P. Serri: "A Model-Based ESL HW/SW Co-Design Framework for Mixed-Criticality Systems", EMC² Summit at CPS Week, Vienna, Austria, 2016
[4] L. Pomante, F. Federici, G. Valente, D. Casalena, D. Andreetti, D. Pascucci. "Exploiting Paravirtualization to Support Time and Space Isolation in Multi-Core Platforms for the Avionic Domain". Euromicro Conference on Digital System Design, 2015

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