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System-Level HW/SW Co-Design Methodology for Real-Time and Mixed Criticality Applications

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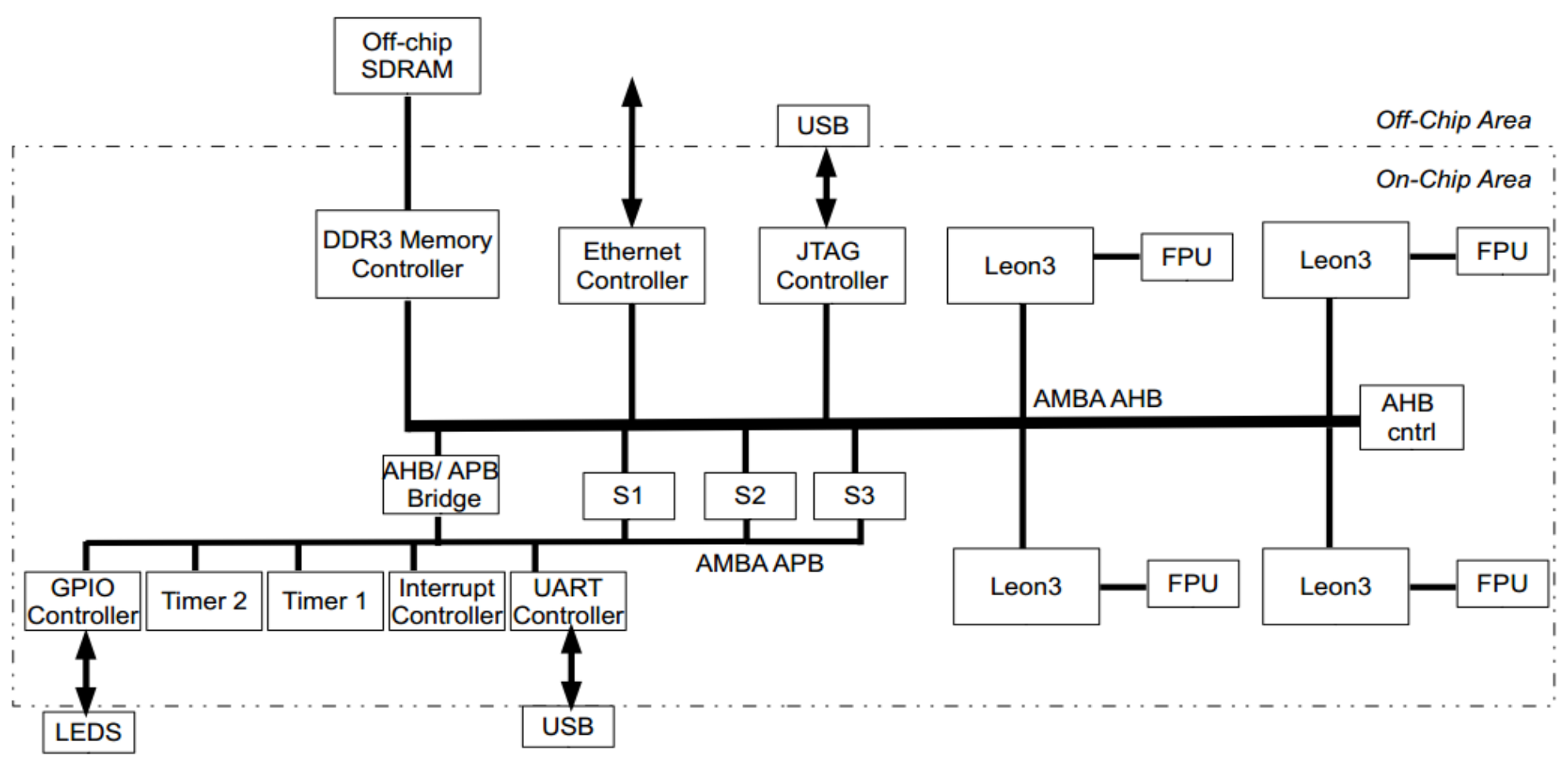
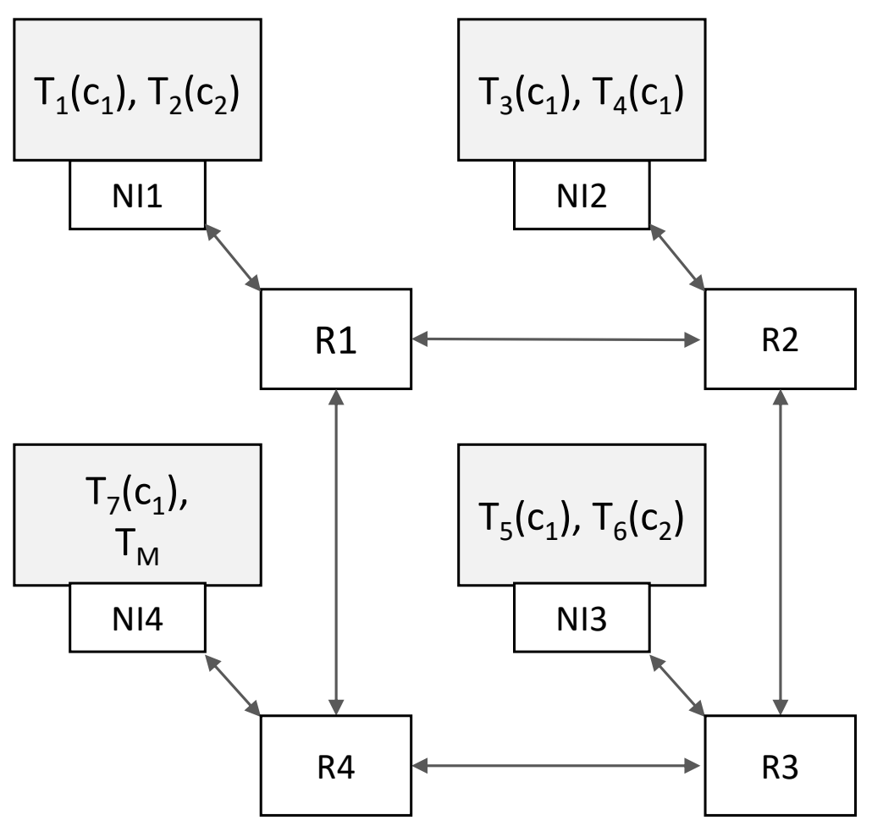
Introduction

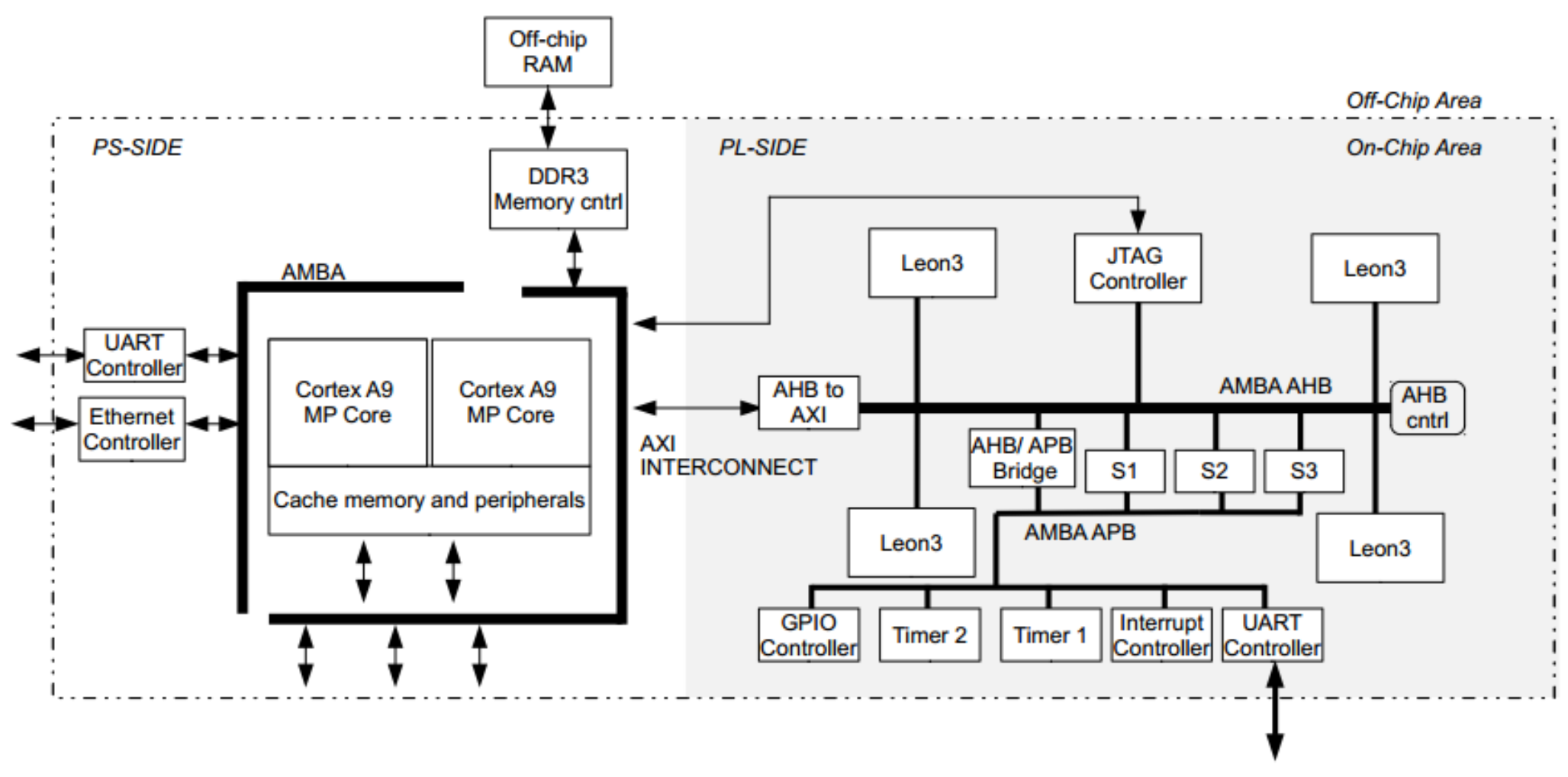
- The early embedded system design activities are to model F/NF requirements and to validate them before final implementation. Designers use system-level models to identify best HW/SW resources allocation by simulating system behavior. Proper SW tools are fundamental to support designers to reduce costs and overall complexity of systems development.
- In such a context, this Ph.D. work is focused on the development of a framework for modeling, analysis and validation of mixed critical systems, through the use of software tools for "*Model-Based ESL HW/SW Co-design*" [1][2], refined to use estimates, metrics and simulations that consider mixed-criticality and real-time requirements, identified in the context of several European project.
- An incremental Electronic System-Level HW/SW Co-Design methodology, and related tools, to design "parallel embedded systems" (e.g. multi-core systems, multi-processor systems, network-on-chip) for mixed-criticality applications has been proposed.
- Starting (at least) from the system behavior specification, timing and mixed-criticality constraints, the proposed approach aims to suggest the HW/SW partitioning, the architecture and the mapping of the partitioned entities onto the HW components into the Design Space Exploration step (i.e. HW/SW partitioning, architecture definition and mapping).

Technologies Background

- Analysis and experimentation of technologies for mixed-criticality support
  - Hypervisors technologies (PikeOS and Xtratum) [3]
  - Ad-hoc HW mechanisms to support isolation in NoC [4]
- Several parallel embedded architectures on FPGA/SoC [5][6] to validate DSE
  - 4-LOOP: 4-(soft)core LEON3 with SMP Linux and OpenMP support (both on Virtex6 FPGA and Zynq7000 SoC)
  - AMP system on Zynq7000 with an "hardwired dual-core ARM running a SMP Linux" that share memory with a "4-(soft)core LEON3 running a SMP Linux"







HepsyCode Methodology

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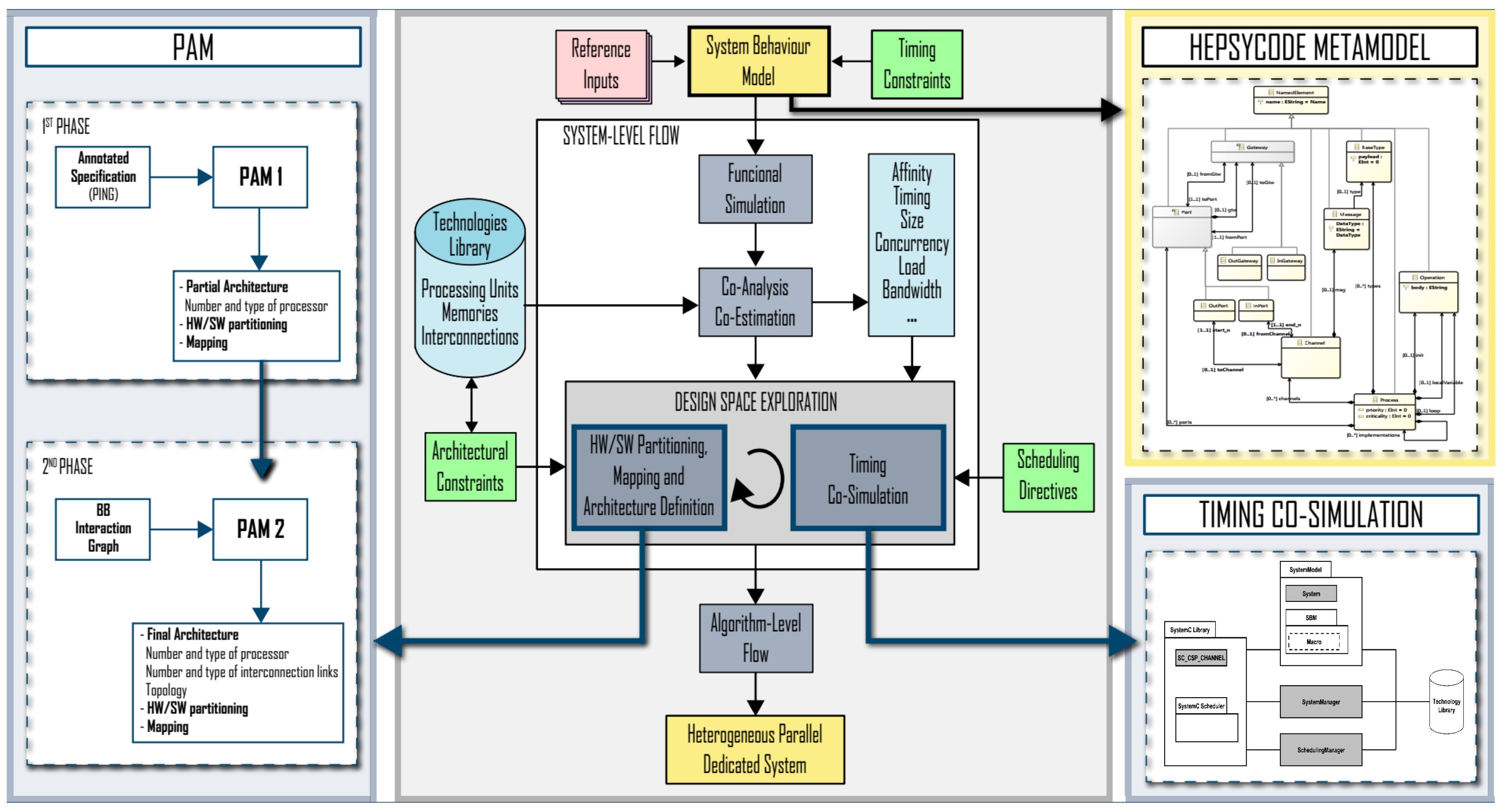
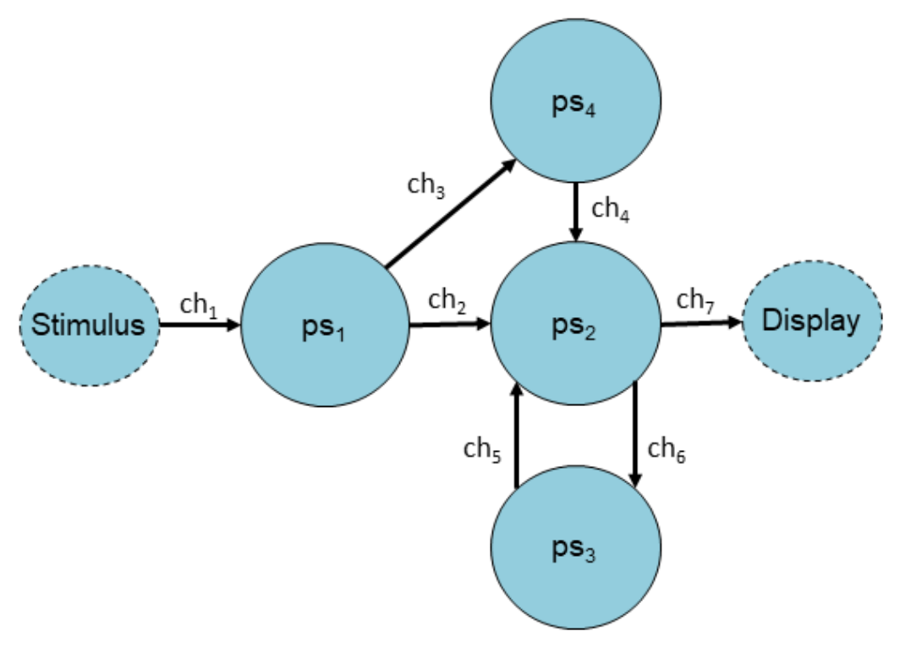
- Application model (CSP-like MoC and SystemC language)
  - CSP processes labeled with criticality and real-time constraints
  - Explicit concurrent and communicating processes
  - Simulatable Model [8][9]

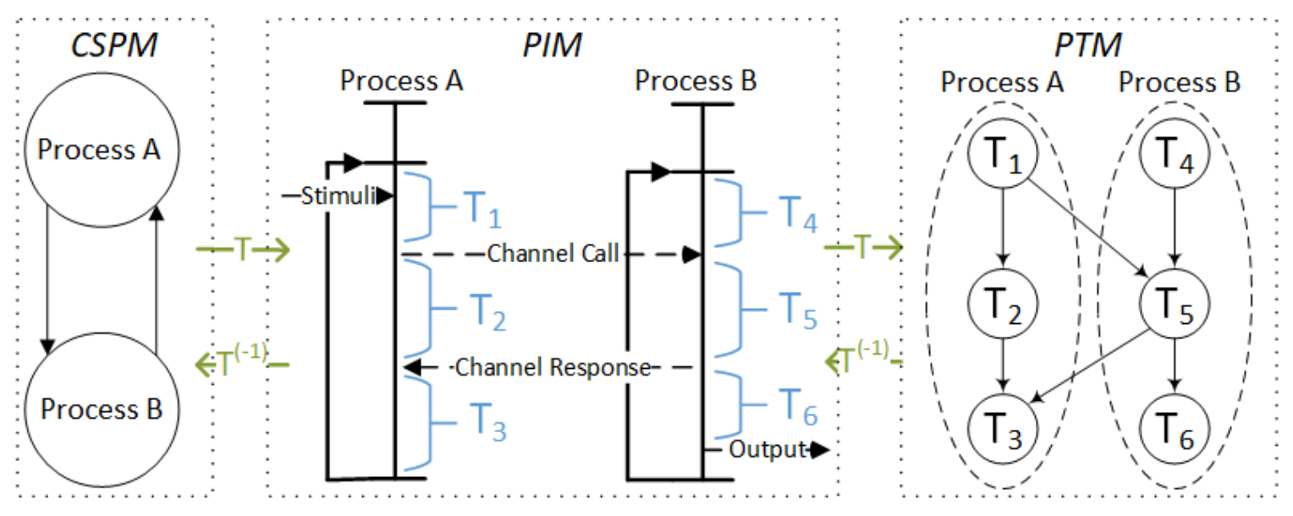


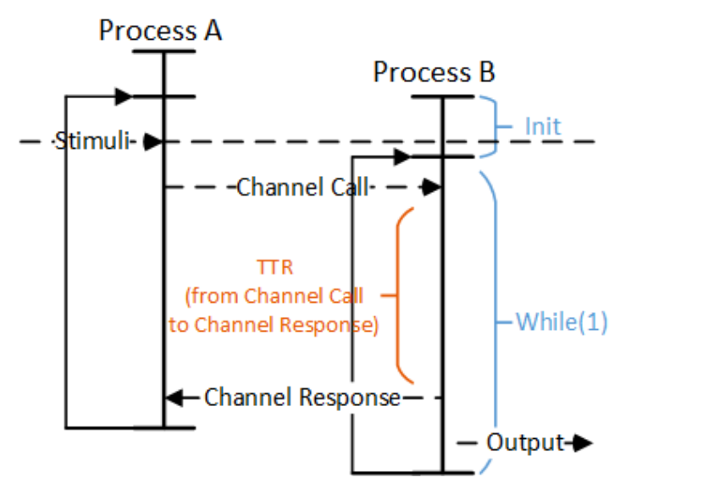
- Basic HW technologies (library describing all HW technologies available for DSE) characterized with respect to relevant features (e.g. performance, power, cost, …)
- Evaluate system-level metrics and estimations in order to drive the DSE by means of an annotated application model

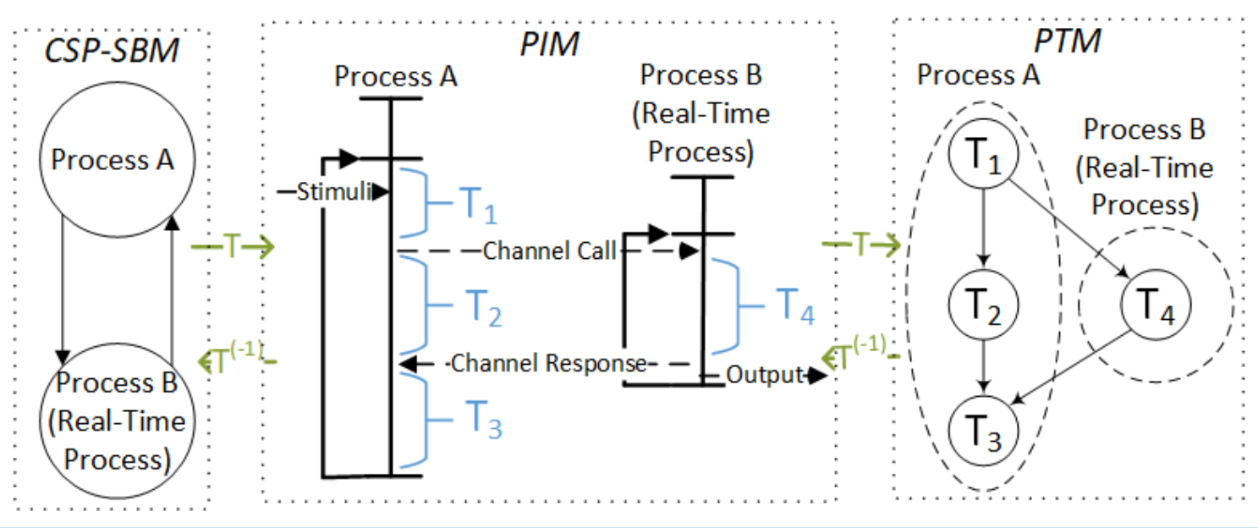
HepsyCode RTMC

- HW/SW support to mixed-critical parallel embedded platforms
- DSE for real-time and mixed-critical parallel embedded platforms
  - Extension of the first-step of the DSE methodology in order to consider also classical RT ones [7]
  - Identification of the main elements to be considered in the second-step of the DSE methodology
  - Extend system-level co-simulation approach to consider also two-levels scheduling policies typically introduced by hypervisors technologies [8]





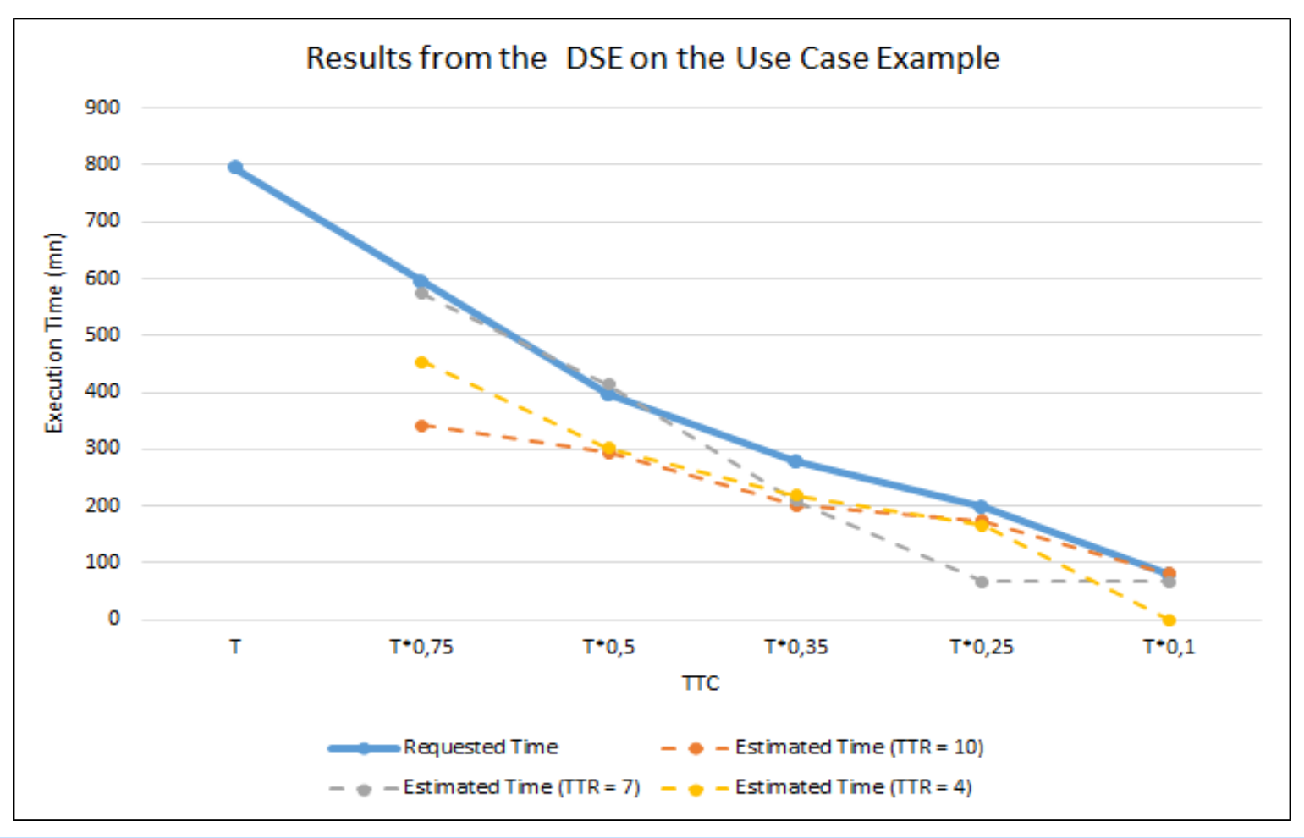




Preliminary Results

Allocation	Simulated Time (ms)	ps_3 (ms)	TTC (ms)	TTR (ms)
All on bb_1	794,88	8,10	600	10
All on bb_2	650,66	5,54	600	10
ps_1, ps_2, ps_3 on bb_1 ps_4 on bb_2,	590,80	8,10	600	10
ps_3 on bb_1 ps_1, ps_4 on bb_2 ps_2 on bb_3	264,89	8,10	400	10
ps_1, ps_3 on bb_1 ps_4 on bb_2 ps_2 on bb_3	298,88	8,10	300	10
ps_4 on bb_1 ps_1, ps_2, ps_3 on bb_3	201,48	0,009	200	10
ps_3 on bb_1 ps_4 on bb_2 ps_1, ps_2 on bb_3	145,67	8,10	200	10
ps_3 on bb_1 ps_1, ps_2, ps_4 on bb_3	81,04	8,10	100	10
ps_1, ps_2 on bb_1 ps_3, ps_4 on bb_2,	562,85	5,54	600	7
ps_1, pu_4 on bb_1 ps_2, ps_3 on bb_2	462,58	5,54	400	7
ps_1 on bb_1 ps_3, ps_4 on bb_2 ps_2 on bb_3	220,80	5,54	400	7
ps_1, on bb_1 ps_3 on bb_2 ps_2, ps_4 on bb_3	206,99	5,54	300	7
ps_3 on bb_2 ps_1, ps_2, ps_4 on bb_3	55,55	5,55	200	7
ps_1, ps_4 on bb_1 ps_2 on bb_2 ps_3 on bb_3	428,87	0,009	600	4
ps_4 on bb_1 ps_1, ps_2 on bb_2 ps_3 on bb_3	337,56	0,009	400	4
ps_4 on bb_1 ps_1 on bb_2 ps_2, ps_3 on bb_3	214,80	0,009	300	4
ps_4 on bb_2 ps_1, ps_2, ps_3 on bb_3	137,62	0,009	200	4
All on bb_3	0,22	0,009	100	4

- **bb_1** (SW-PU): 20 MHz 8-bit 8051 CISC core with 128 byte of Internal RAM, 64K of internal ROM, without cache and external memory (cost 10);
- **bb_2** (SW-PU): 150 MHz 32-bit LEON3 soft-processor with 2*4 KiB L1 caches, RAM size of 4096 KiB and a ROM of 2048 KiB (cost 50);
- **bb_3** (HW-PU): 300 MHz Altera Stratix V (cost 300).



- Experimentation of enabling technologies for mixed-criticality support that have been considered as building blocks to be exploited during DSE to provide mixed-criticality support to parallel architectures
- Customized the general DSE methodology to exploit hypervisor technologies
- Contributed to benchmarking of fully-open Aeroflex Gaisler quad-LEON3 system on FPGA with Xtratum and PikeOS

Conclusion and Future Work

- This work propose an extended and ESL Electronic Design Automation methodology (and related tools) to help designers to develop Mixed-Criticality and Real-time Embedded Systems.
- Other than on basic RT constraints, this work focuses also on mixed-criticality ones. For this, the DSE step will try also to group processes with the same level of criticality on the same processor/partition. Then, a two-levels scheduling is considered during co-simulation to model possible hypervisor technologies. Finally an extensible database of hardware components (called Technology Library) is provided to designer in order to identify the best platform to satisfy F/NF constraints.
- Future works involves model GR-CPCI-LEON4-N2X Quad-Core 32-bit LEON4 SPARC V8 processor with MMU, IOMMU and TASI/UNIVAQ Satellite Application
- This work has been partially supported by the ECSEL RIA 2016 **MegaM@Rt²** (https://megamart2-ecsel.eu) and **AQUAS** (http://aquas-project.eu) European Projects

Reference

[1] L. Pomante, "HW/SW co-design of dedicated heterogeneous parallel systems: an extended design space exploration approach," Computers & Digital Techniques, IET, vol.7, no.6, pp.246,254, 2013
[2] L. Pomante, C. Bolchini, F. Salice, D. Sciuto. "Reliability Properties Assessment at System Level: a Co-Design Framework", Journal of Electronic Testing - Theory and Application (JETTA), Kluwer Academic Publishers, The Netherlands, Vol. 18, no. 3, p. 351-356, 2002.
[3] L. Pomante, C. Tieri, F. Federici, M. Colizza, M. Faccio, R. Cardinali, B. Iorio. "HW Mechanisms to Support Isolation in Mixed-Criticality NoC". Euromicro Conference on Digital System Design, 2014
[4] L. Pomante, F. Federici, G. Valente, D. Casalena, D. Andreetti, D. Pascucci. "Exploiting Paravirtualization to Support Time and Space Isolation in Multi-Core Platforms for the Avionic Domain". Euromicro Conference on Digital System Design, 2015
[5] L. Pomante, V. Muttillo, G. Valente, F. Federici, M. Faccio, C. Tieri. "Enhancing an FPGA-Based SMP Embedded Platform with OpenMP Support and Unobtrusive System Monitor". Euromicro Conference on Digital System Design, 2015
[6] L. Pomante, V. Muttillo, G. Valente, F. Federici, M. Faccio. "4-LOOP: 4-core Leon3 with Linux operating system, OpenMP library and hardware profiling system". Conference on Design and Test Automation in Europe (DATE) – University Booth, 2015
[7] L. Pomante, V. Muttillo, G. Valente, F. Federici, P. Serri: "A Model-Based ESL HW/SW Co-Design Framework for Mixed-Criticality Systems", EMC² Summit at CPS Week, Vienna, Austria, 2016
[8] D. Ciambrone, V. Muttillo, G. Valente, L. Pomante, "HW/SW Co-Simulator for Embedded Heterogeneous Parallel Systems", Euromicro Conference on Digital Systems Design (DSD) - Work in Progress Session, 2017
[9] V. Stoico, V. Muttillo, G. Valente, L. Pomante, F. D'Antonio, "CC4CS: A Unifying Statement-Level Performance Metric for HW/SW Technologies", Euromicro Conference on Digital Systems Design (DSD) - Work in Progress Session, 2017

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