System-Level HW/SW Co-Design Methodology for Real-Time and Mixed Criticality Applications

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***Vittoriano Muttillo**, Giacomo Valente, Luigi Pomante*

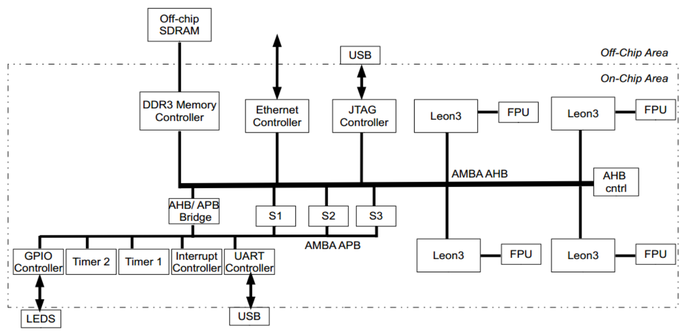
University of L'Aquila ITALY

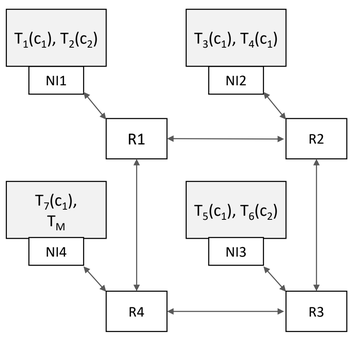
Introduction

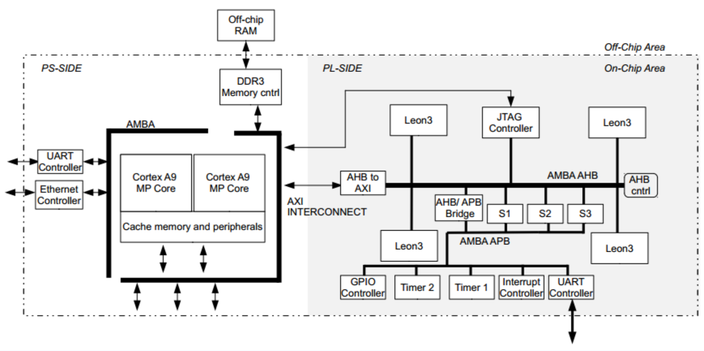
- The early embedded system design activities are to model F/NF requirements and to validate them before final implementation. Designers use system-level models to identify best HW/SW resources allocation by simulating system behavior. Proper SW tools are fundamental to support designers to reduce costs and overall complexity of systems development.
- In such a context, this Ph.D. work is focused on the development of a framework for modeling, analysis and validation of mixed critical systems, through the use of software tools for "*Model-Based ESL HW/SW Co-design*" [1][2], refined to use estimates, metrics and simulations that consider mixed-criticality and real-time requirements, identified in the context of several European project.
- An incremental Electronic System-Level HW/SW Co-Design methodology, and related tools, to design "parallel embedded systems" (e.g. multi-core systems, multi-processor systems, network-on-chip) for mixed-criticality applications has been proposed.
- Starting (at least) from the system behavior specification, timing and mixed-criticality constraints, the proposed approach aims to suggest the HW/SW partitioning, the architecture and the mapping of the partitioned entities onto the HW components into the Design Space Exploration step (i.e. HW/SW partitioning, architecture definition and mapping).

Technologies Background

- Analysis and experimentation of technologies for mixed-criticality support
  - Hypervisors technologies (PikeOS and Xtratum) [3]
  - Ad-hoc HW mechanisms to support isolation in NoC [4]
- Several parallel embedded architectures on FPGA/SoC [5][6] to validate DSE
  - 4-LOOP: 4-(soft)core LEON3 with SMP Linux and OpenMP support (both on Virtex6 FPGA and Zynq7000 SoC)
  - AMP system on Zynq7000 with an "hardwired dual-core ARM running a SMP Linux" that share memory with a "4-(soft)core LEON3 running a SMP Linux"



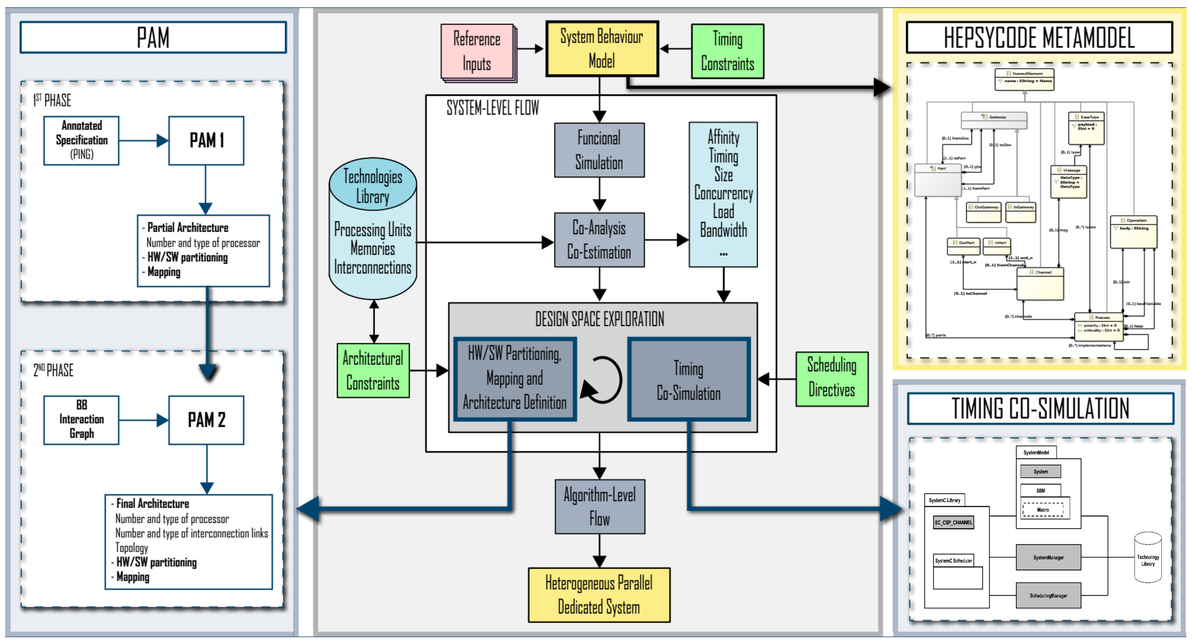




HepsyCode Methodology

- Application model (CSP-like MoC and SystemC language)
  - CSP processes labeled with criticality and real-time constraints
  - Explicit concurrent and communicating processes
  - Simulatable Model [8][9]

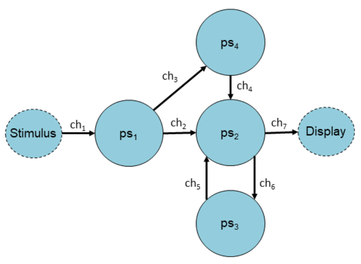
www.hepsycode.com

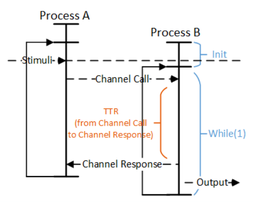


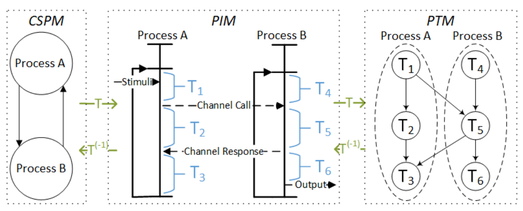
- Basic HW technologies (library describing all HW technologies available for DSE) characterized with respect to relevant features (e.g. performance, power, cost, …)
- Evaluate system-level metrics and estimations in order to drive the DSE by means of an annotated application model

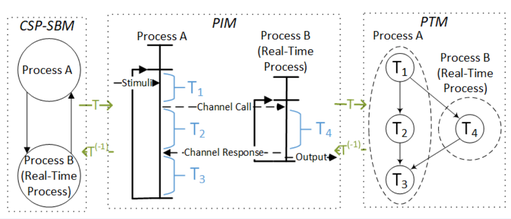
HepsyCode RTMC

- HW/SW support to mixed-critical parallel embedded platforms
- DSE for real-time and mixed-critical parallel embedded platforms
  - Extension of the first-step of the DSE methodology in order to consider also classical RT ones [7]
  - Identification of the main elements to be considered in the second-step of the DSE methodology
  - Extend system-level co-simulation approach to consider also two-levels scheduling policies typically introduced by hypervisors technologies [8]





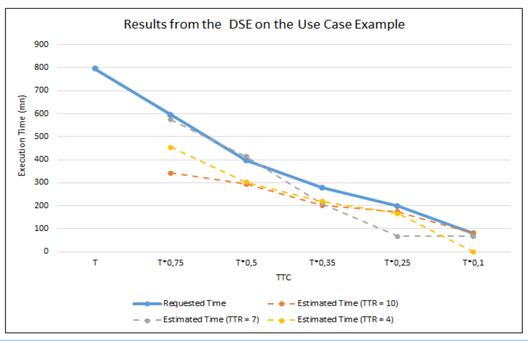




Preliminary Results

Allocation	Simulated Time (ms)	ps3 (ms)	TTC (ms)	TTR (ms)
All on bb1	794,88	8,10	600	10
All on bb2	650,66	5,54	600	10
ps1, ps2, ps3 on bb1 ps4 on bb2,	590,80	8,10	600	10
ps1 on bb1 ps2, ps4 on bb2 ps3 on bb3	264,89	8,10	400	10
ps1, ps2 on bb1 ps4 on bb2 ps3 on bb3	298,88	8,10	300	10
ps4 on bb1 ps1, ps2, ps3 on bb2	201,48	0,009	200	10
ps1 on bb1 ps4 on bb2 ps2, ps3 on bb3	145,67	8,10	200	10
ps1 on bb1 ps1, ps2, ps4 on bb2 ps1, ps2 on bb3 ps3 on bb4,	81,04	8,10	100	10
ps1, ps4 on bb1 ps2, ps3 on bb2	562,85	5,54	600	7
ps1, ps4 on bb1 ps2, ps3 on bb2	462,58	5,54	400	7
ps1 on bb1 ps2, ps4 on bb2 ps3 on bb3	220,80	5,54	400	7
ps1, on bb1 ps3 on bb2 ps2, ps4 on bb3	206,99	5,54	300	7
ps3 on bb2 ps1, ps2, ps4 on bb1 ps1, ps4 on bb3 ps2 on bb4 ps3 on bb5	55,55	5,55	200	7
ps4 on bb1 ps2, ps3 on bb2 ps1 on bb3	428,87	0,009	600	4
ps4 on bb1 ps1, ps2 on bb2 ps3 on bb3	337,56	0,009	400	4
ps4 on bb1 ps1 on bb2 ps2, ps3 on bb3	214,80	0,009	300	4
ps4 on bb2 ps1, ps2, ps3 on bb1	137,62	0,009	200	4
All on bb3	0,22	0,009	100	4

- **bb$_1$** (SW-PU): 20 MHz 8-bit 8051 CISC core with 128 byte of Internal RAM, 64K of internal ROM, without cache and external memory (cost 10);
- **bb$_2$** (SW-PU): 150 MHz 32-bit LEON3 soft-processor with 2*4 KiB L1 caches, RAM size of 4096 KiB and a ROM of 2048 KiB (cost 50);
- **bb$_3$** (HW-PU): 300 MHz Altera Stratix V (cost 300).



- Experimentation of enabling technologies for mixed-criticality support that have been considered as building blocks to be exploited during DSE to provide mixed-criticality support to parallel architectures
- Customized the general DSE methodology to exploit hypervisor technologies
- Contributed to benchmarking of fully-open Aeroflex Gaisler quad-LEON3 system on FPGA with Xtratum and PikeOS

Conclusion and Future Work

- This work propose an extended and ESL Electronic Design Automation methodology (and related tools) to help designers to develop Mixed-Criticality and Real-time Embedded Systems.
- Other than on basic RT constraints, this work focuses also on mixed-criticality ones. For this, the DSE step will try also to group processes with the same level of criticality on the same processor/partition. Then, a two-levels scheduling is considered during co-simulation to model possible hypervisor technologies. Finally an extensible database of hardware components (called Technology Library) is provided to designer in order to identify the best platform to satisfy F/NF constraints.
- Future works involves model GR-CPCI-LEON4-N2X Quad-Core 32-bit LEON4 SPARC V8 processor with MMU, IOMMU and TASI/UNIVAQ Satellite Application
- This work has been partially supported by the ECSEL RIA 2016 **MegaM@Rt²** (https://megamart2-ecsel.eu) and **AQUAS** (http://aquas-project.eu) European Projects

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Contact author {vittoriano.muttillo, giacomo.valente}@graduate.univaq.it, luigi.pomante@univaq.it
DEWS Center of Excellence, University of L'Aquila, Italy (http://dews.univaq.it)
DISIM Department of Information Engineering, Computer Science and Mathematics (http:// www.disim.univaq.it)