A Real-Time and Mixed Criticality Extension for a System-Level HW/SW Co-Design Methodology

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Introduction

- The early embedded system design activities are to model F/NF requirements and to validate them before final implementation.
- Designers use system-level models to identify best HW/SW resources allocation by simulating system behavior.
- Proper SW tools are fundamental to support designers to reduce costs and overall complexity of systems development.

Background

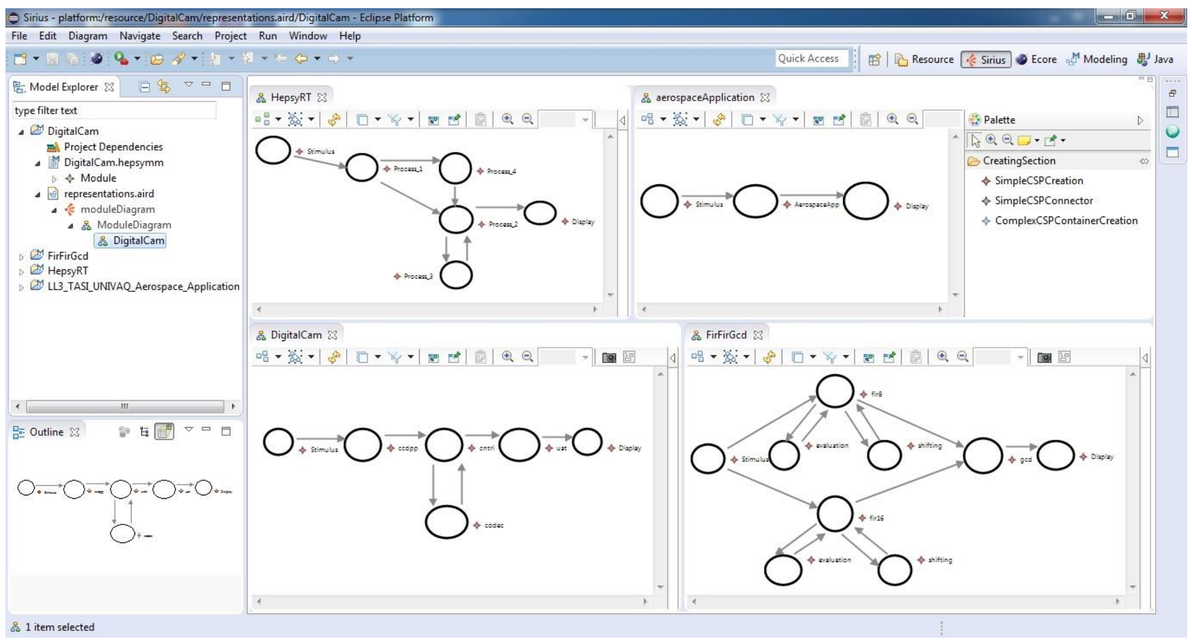
- **Mixed-Critical Systems** [1], run multiple applications with different criticality-levels on the same HW/SW platform (industrial challenge).
- The system is designed in order to guarantee space/time isolation.
- The use of multi/many-core embedded platforms can improve systems performance.

Goals

- Proposed project is focused on the development of a framework for modeling, analysis and validation of mixed critical systems, through the use of software tools for "**Model-Based ESL HW/SW Co-design**", refined to use estimates, metrics and simulations that consider mixed-criticality and real-time requirements, identified in the context of the **EMC² Artemis-JU AIPP** [2] European research project.

HEPSYCODE-RT

GRAPHICAL USER INTERFACE



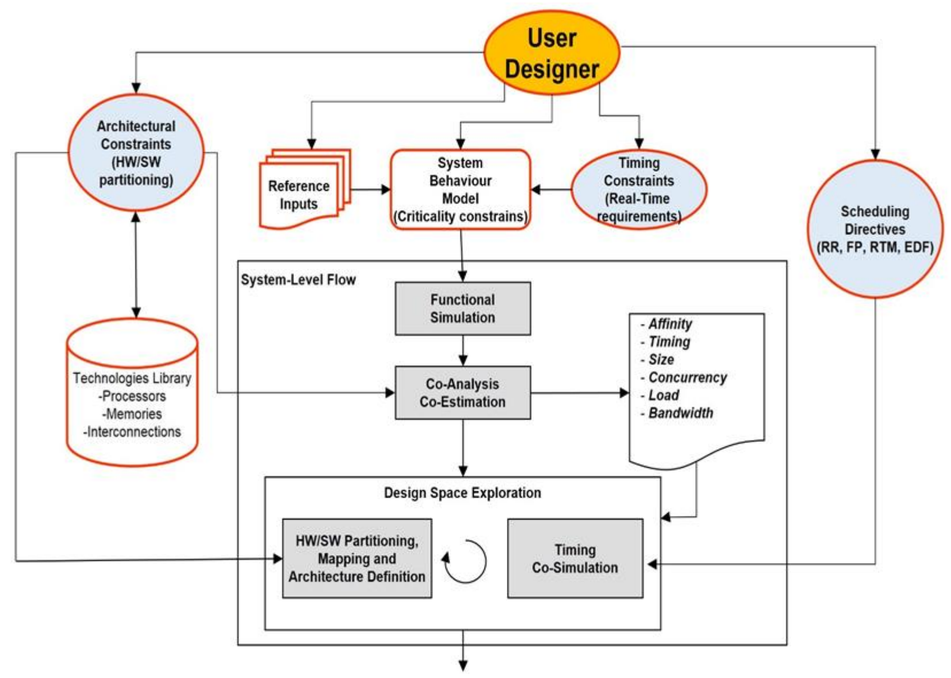
The GUI involves Eclipse Modeling Framework (EMF) plugins:

- **Sirius** technologies, to create custom graphical modeling workbenches by leveraging the Eclipse tool
- **Acceleo** Object Management Group (OMG) Meta-Object Facility (MOF) Model to Text Language (MTL) for model transformation from CSP-like to SystemC.

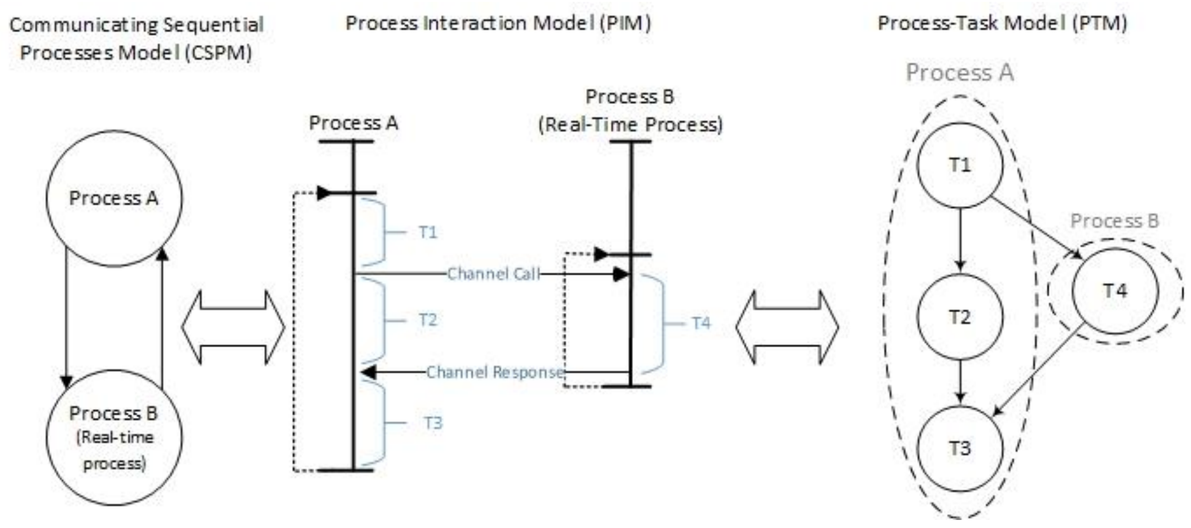
MODELING LANGUAGE & PING MODEL

- The System Behavioral Model (SBM) is based on the **Communication Sequential Processes** (CSP) model of computation [3].
- A proper HW/SW Modeling Language (HML) is used as an input for a Model to Model (M2M) transformation
- **Procedural INteraction Graph** (PING), has been adopted to internally represent system specification

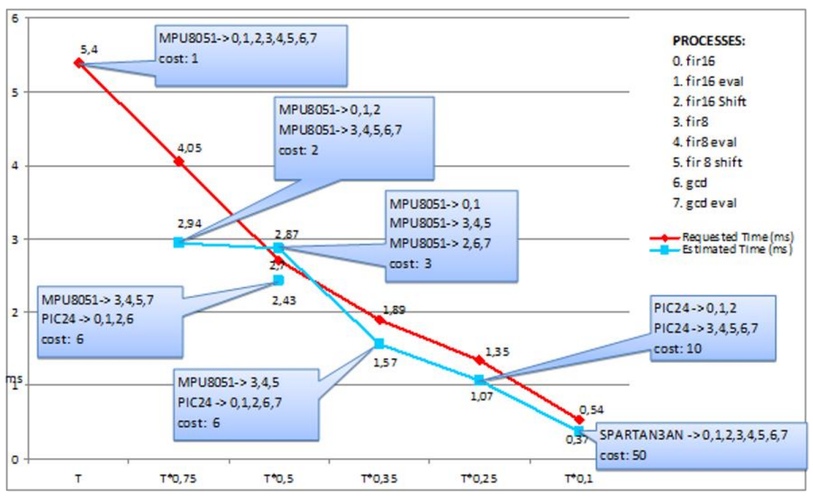
SYSTEM-LEVEL FLOW [4]



REAL-TIME EXTENSION



Test



Recent Works

Other than on basic RT constraints, this work focuses also on mixed-criticalty ones. For this, the DSE step will try also to group processes with the same level of criticality on the same processor/partition. Then, a two-levels scheduling is considered during co-simulation to model possible hypervisor technologies. Finally an extensible database of hardware components (called *Technology Library*) is provided to designer in order to identify the best platform to satisfy F/NF constraints.

Future Works

This work propose an extended and innovative **ESL *Eletronic Design Automation*** methodology to help designers to develop Mixed-Criticality and Real-time Embedded Systems. Moreover, being related to the EMC2 project, there is need to improve the methodology using WP and Living Lab results. Hopefully, the final methodology will be able to suggest both the HW platform and the HW/SW mapping for specific application, and could be used in other European Projects (AQUAS).

Reference:
[1] Burns, Alan, and Robert Davis. "Mixed criticality systems-a review." Department of Computer Science, University of York, Tech. Rep (2013)
[2] Artemis-JU AIPP EMC2, http://www.artemis-emc2.eu/
[3] Hoare, Charles Antony Richard. "Communicating sequential processes."*Communications of the ACM* 21.8 (1978): 666-677
[4] Pomante, Luigi. "System-level design space exploration for dedicated heterogeneous multi-processor systems." Application-Specific Systems, Architectures and Processors (ASAP), IEEE International Conference on. (2011)

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