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Work-In-Progress: Cyber-Physical Systems and Dynamic Partial Reconfiguration Scalability: opportunities and challenges

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THE PROPOSED WORK

The Dynamic Partial Reconfiguration process

- The DPR is a Field Programmable Gate Arrays (FPGAs) process that allows, at run-time, the reconfiguration of a HW portion while the remainder of the processes stay operative and unaffected.
- The DPR is useful to enable the systems (e.g, CPSs) to autonomously adapt their hardware configuration to the environment changes, also in the presence of hard real-time constraints.
- The DPR has been improved during the years reducing the reconfiguration file granularity and increasing the number of DPR requests.

Our Work

- A theoretical and practical investigation on the number of DPR requests (i.e., DPR scalability) that a dynamic reconfiguration controller can be efficiently managed in the hard real-time systems.
  - The theoretical investigation has been conducted using the only framework, in the hard real-time systems, that allows the DPR scalability usage.
  - The practical investigation has been conducted identifying and using an existing dynamic reconfiguration controller that supports the DPR scalability.