Work-In-Progress: Cyber-Physical Systems and Dynamic Partial Reconfiguration Scalability: opportunities and challenges

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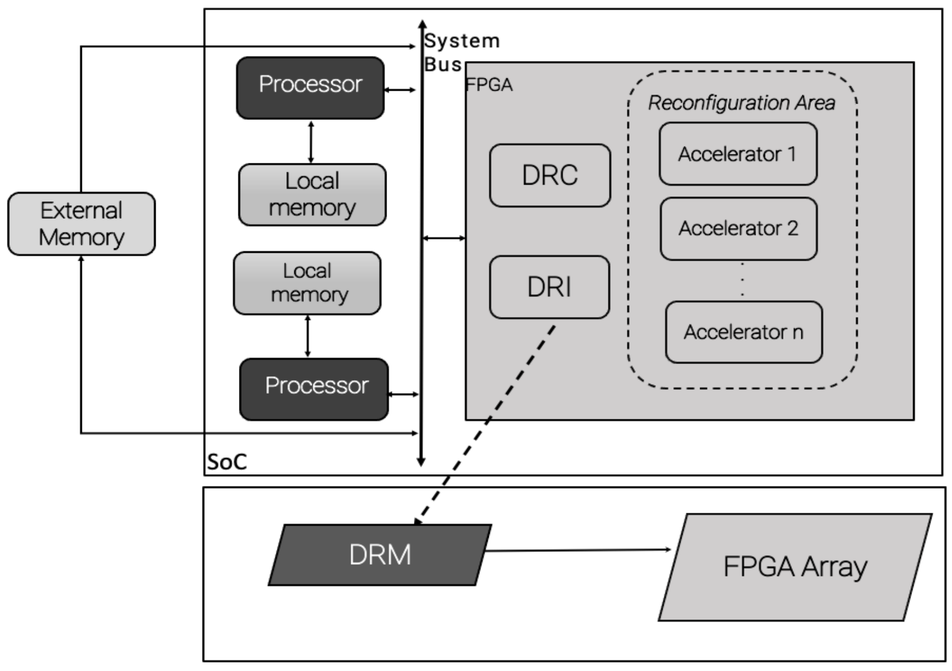
The Dynamic Partial Reconfiguration Process

DPR Main Concepts

The DPR process:

- allows to reconfigure, at run-time, a portion of HW while the remainder of the process continues to operate;
- requires a certain amount of time to apply the reconfiguration;
- can be considered established only when a **reconfiguration file (BS)** is loaded within the **Dynamic Reconfiguration Memory (DRM).**

DPR Reference platform and involved components

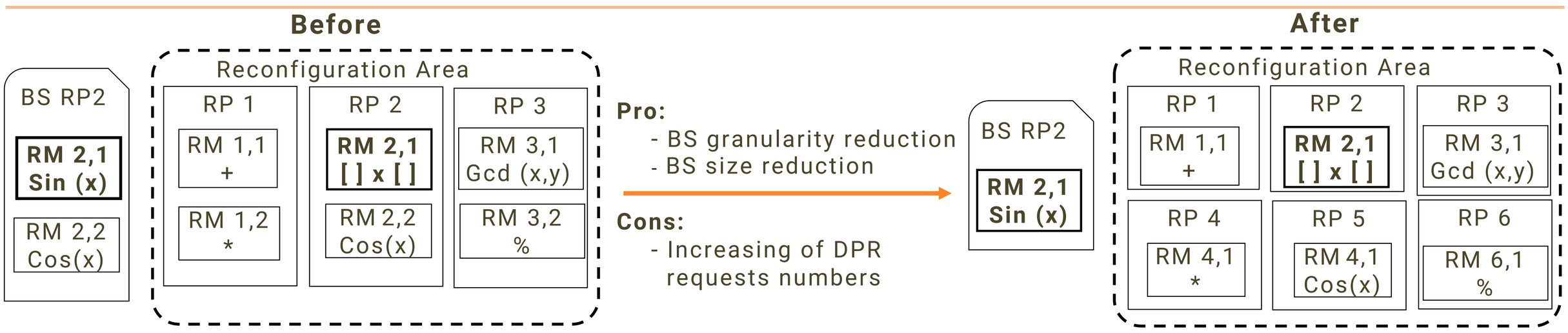


DPR Main Steps

1. The processor system moves the reconfiguration file (BS) from an external memory to its local memory.
2. The processor moves the BS from its local memory to **Dynamic Reconfiguration Interface (DRI),** through a **Dynamic Reconfiguration Controller (DRC).**
3. The DRI moves the BS to the DRM.

The Evolution of Dynamic Partial Reconfiguration

Example: DPR usage to modify the current implementation of the **reconfiguration module (RM)** 2,1 belonging to the **reconfiguration partition (RP 2)** 2.

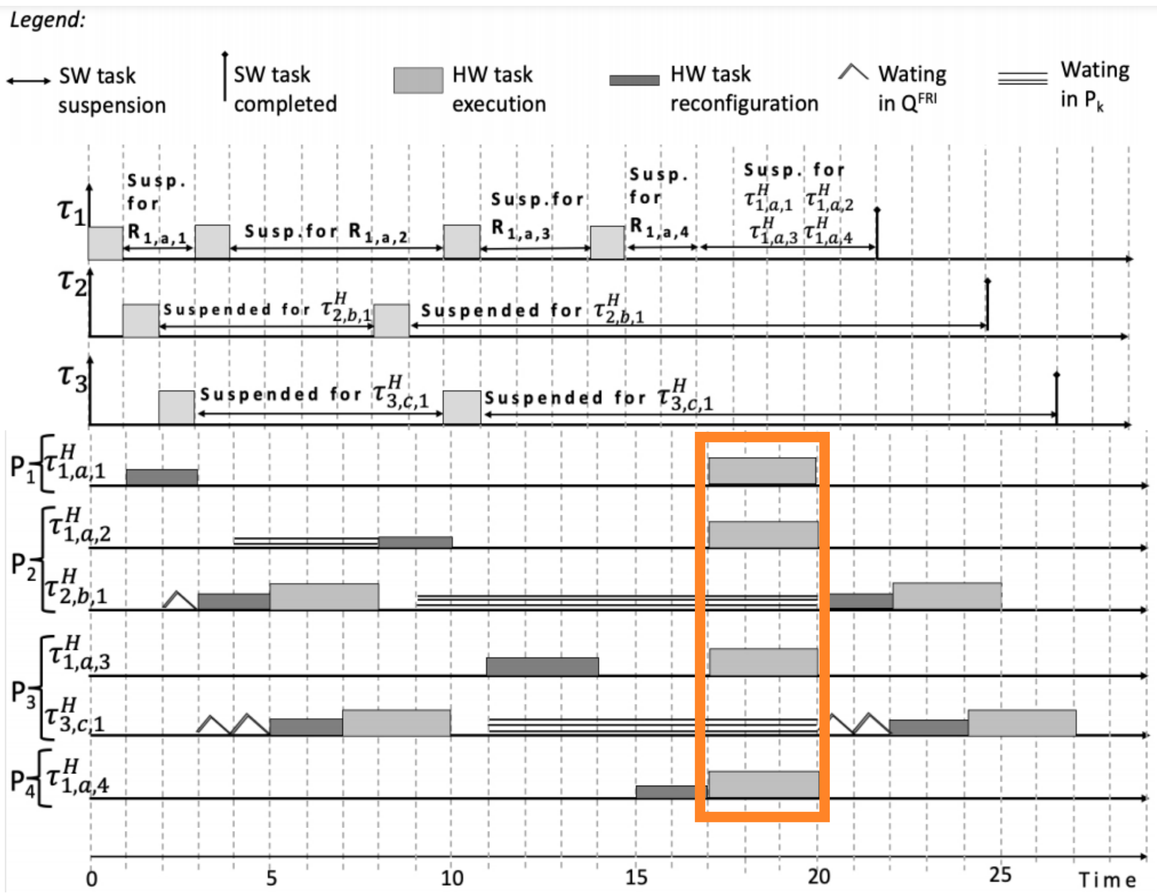


Open Issue: Is the DPR process scalable in the hard real-time systems (i.e., Are there existing DRCs in the hard real-time systems able to efficiently handle multiple DPR requests)?

DPR scalability – theoretical investigation

Theoretical Investigation:

- It is based on FRED*, the only framework in hard real-time literature, that does not explicitly exclude the DPR scalability adoption.



DPR scalability – Practical investigation

Controller	DMA	Scalability
Xilinx PCAP Zynq-7000	YES	N.D
Xilinx PCAP Zynq-Ultrascale	YES	N.D
Xilinx MCAP-based	YES	YES
Xilinx ICAP-based	NO	NO
Intel PR	NO	NO
ZyCAP controller	YES	NO
ICAP intelligent controller	YES	NO
PLB ICAP controller	YES	NO
CoRQ controller	YES	NO
RT-ICAP controller	NO	NO
A Partial Reconfiguration Controller for Altera Stratix V FPGAs	NO	No
FSL ICAP	NO	NO

Experi-mentation

pBS Number	pBS Name	Total pBS size (KB)	Application Output	Measured RT (ms)	Expected RT (ms)
1	add.bin	110.984	✓	0.69469	0.85341
2	add.bin mult.bin	221.968	✓	1.38938	1.70682
3	add.bin mult.bin add.bin	332.952	✗	1.38938	2.56023
4	add.bin mult.bin add.bin mult.bin	442.952	✗	1.38938	3.41364

Result:

- The theoretical investigation proves that FRED supports the DPR scalability but some modifications have been necessary to manage multiple DPR requests and obtain a bounded response time.

Result:

- The practical investigation proves that the Xilinx PCAP Zynq-7000 controller supports the DPR scalability even if has been found an unknown limit on the number of DPR requests that this controller can efficiently manage. Has been found that the Xilinx PCAP Zynq-7000 controller can support two DPR requests per time.

Future Works:

- To produce a revision of FRED to verify if it is possible to adequately consider the DPR scalability feature.
- To produce a new implementation to overcome the discovered DPR scalability limit.

* A. Biondi, A. Balsini, M. Pagani, E. Rossi, M. Marinoni, and G. Buttazzo, "A framework for supporting real-time applications on dynamic reconfigurable fpgas," in IEEE Real-Time Systems Symposium (RTSS), Nov. 2016, pp. 1–12

Acknowledgements: This work has been partially supported by the **ECSEL RIA 2017 FITOPTIVIS GA 783162**